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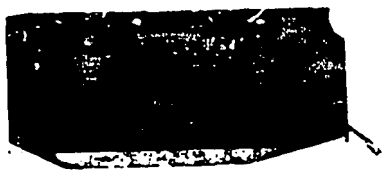

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3-11-94	1.	Application ✓ papers.	
	2.	Pre-Amdt A	12-29-93
	3.	Prior Art	Dec 22, 1994
1/4/95	4.	Pre-Amdt B	Dec 22, 1994
	5.	Prior Art	1-9-95
	6.	Prior Art	Jan 17, 1995
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4/17	8.	Rej. (3)	5-15-95
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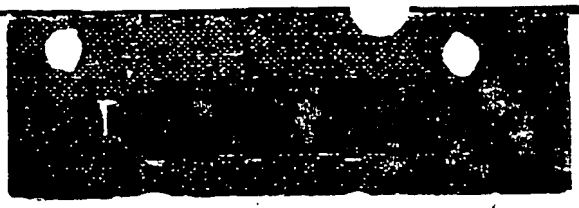

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DATE	CLASS	SUBCLASS	GROUP ART	EXAMINER
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APPL: ARI, LOS GATOS, CA; ROBERT P. NORMAN, SAN JOSE, CA; SANJAY ILPITAS, CA.

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FLASH EEPROM SYSTEM

U.S. DEPT. of COMM./Pat. & TM Office — PTO-436L (rev. 10

PARTS OF APPLICATION FILED SEPARATELY

W. Lee 8/21/96
Applications Examiner

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
AUG 20 1996	Ly V. Hua	Total Claims: 50	Print Claim: 1

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POSITION		ID NO.	DATE
CLASSIFIER			2-1-94
EXAMINER		230	2-2-94
TYPIST		330	2/5
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CORPS CORR.			
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INDEX OF CLAIMS

Claim Final	Claim Original	11/3/95	8/16/96
	1	100 ✓	
	2	101 ✓	
	3	102 ✓	
	4	103 ✓	
	5	104 ✓	
	6	105 ✓	
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SYMBOLS

✓ ..... Rejected
= ..... Allowed
- (Through numeral) Canceled
+ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

Claim Final	Claim Original	11/15/95	8/16/96
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SEARCHED

Class	Sub.	Date	Exmr.
371	10.2	4/5/95	EWL
"	10.3	4/5/95	EWL
"	40.1	4/5/95	EWL
365	200	4/5/95	EWL
395	575	4/6/95	EWL
395	182.03	11/7/95	EWL
395	182.04	11/7/95	EWL
395	182.05	11/7/95	EWL
395	182.06	11/7/95	EWL
365	185.09	11/8/95	EWL
365	200	11/8/95	EWL
365	201	11/8/95	EWL
365	189.07	11/8/95	EWL
Update	above	8/14/96	EWL
395	427	8/14/96	EWL
395	430	8/14/96	EWL

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
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SEARCH NOTES

	Date	Exmr.
AFS Search	4/7/95	EWL

(RIGHT OUTSIDE)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR PATENT

Title: FLASH EEprom SYSTEM
Inventors: Eliyahou Harari, Robert D. Norman, Sanjay Mehrotra

clm A1

Background of the Invention

This invention relates generally to semiconductor electrically erasable programmable read only memories (EEprom), and specifically to a system of integrated circuit Flash EEprom chips.

Computer systems typically use magnetic disk drives for mass storage of data. However, disk drives are disadvantageous in that they are bulky and in their requirement for high precision moving mechanical parts. Consequently they are not rugged and are prone to reliability problems, as well as consuming significant amounts of power. Solid state memory devices such as DRAM's and SRAM's do not suffer from these disadvantages. However, they are much more expensive, and require constant power to maintain their memory (volatile). Consequently, they are typically used as temporary storage.

EEprom's and Flash EEprom's are also solid state memory devices. Moreover, they are nonvolatile, and retain their memory even after power is shut down. However, conventional Flash EEprom's have a limited lifetime in terms of the number of write (or program)/erase cycles they can endure. Typically the devices are rendered unreliable after 10^2 to 10^3 write/erase cycles. Traditionally, they are typically used in applications where semi-permanent storage of data or program is required but with a limited need for reprogramming.

Accordingly, it is an object of the present invention to provide a Flash EEprom memory system with enhanced performance and which remains reliable after enduring a large number of write/erase cycles.

It is another object of the present invention to provide an improved Flash EEprom system which can serve as non-volatile memory in a computer system.

It is another object of the present invention to provide an improved Flash EEprom system that can replace magnetic disk storage devices in computer systems.

It is another object of the present invention to provide a Flash EEprom system with improved erase operation.

It is another object of the present invention to provide a Flash EEprom system with improved error correction.

It is yet another object of the present invention to provide a Flash EEprom with improved write operation that minimizes stress to the Flash EEprom device.

It is still another object of the present invention to provide a Flash EEprom system with enhanced write operation.

Summary of the Invention

These and additional objects are accomplished by improvements in the architecture of a system of EEprom chips, and the circuits and techniques therein.

According to one aspect of the present invention, an array of Flash EEprom cells on a chip is organized into sectors such that all cells within each sector are erasable at once. A Flash EEprom memory system comprises one or more Flash EEprom chips under the control of a controller. The invention allows any

combination of sectors among the chips to be selected and then erased simultaneously. This is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation. This feature is important for stopping those sectors that are first to be erased correctly to the "erased" state from over erasing, thereby preventing unnecessary stress to the Flash EEprom device. The invention also allows a global de-select of all sectors in the system so that no sectors are selected for erase. This global reset can quickly put the system back to its initial state ready for selecting the next combination of sectors for erase. Another feature of the invention is that the selection is independent of the chip select signal which enables a particular chip for read or write operation. Therefore it is possible to perform an erase operation on some of the Flash EEprom chips while read and write operations may be performed on other chips not involved in the erase operation.

According to another aspect of the invention, improved error correction circuits and techniques are used to correct for errors arising from defective Flash EEprom memory cells. One feature of the invention allows defect mapping at cell level in which a defective cell is replaced by a substitute cell from the same sector. The defect pointer which connects the address of the defective cell to that of the substitute cell is stored in a defect map. Every time the defective cell is accessed, its bad data is replaced by the good data from the substitute cell.

Another feature of the invention allows defect mapping at the sector level. When the number of

defective cells in a sector exceeds a predetermined number, the sector containing the defective cells is replaced by a substitute sector.

An important feature of the invention allows defective cells or defective sectors to be remapped as soon as they are detected thereby enabling error correction codes to adequately rectify the relatively few errors that may crop up in the system.

According to yet another aspect of the present invention, a write cache is used to minimize the number of writes to the Flash EEprom memory. In this way the Flash EEprom memory will be subject to fewer stress inducing write/erase cycles, thereby retarding its aging. The most active data files are written to the cache memory instead of the Flash EEprom memory. Only when the activity levels have reduced to a predetermined level are the data files written from the cache memory to the Flash EEprom memory. Another advantage of the invention is the increase in write throughput by virtue of the faster cache memory.

According to yet another aspect of the present invention, one or more printed circuit cards are provided which contain controller and EEprom circuit chips for use in a computer system memory for long term, non-volatile storage, in place of a hard disk system, and which incorporate various of the other aspects of this invention alone and in combination.

Additional objects, features, and advantages of the present invention will be understood from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Fig. 1A is a general micrprocessor system including the Flash EEprom memory system of the present invention;

Fig. 1B is schematic block diagram illustrating a system including a number of Flash EEprom memory chips and a controller chip;

Fig. 2 is a schematic illustration of a system of Flash EEprom chips, among which memory sectors are selected to be erased;

Fig. 3A is a block circuit diagram ~~in the controller~~ for implementing selective multiple sector erase according to the preferred embodiment;

Fig. 3B shows details of a typical register used to select a sector for erase as shown in Fig. 2A;

Fig. 4 is a flow diagram illustrating the erase sequence of selective multiple sector erase;

Fig. 5 is a schematic illustration showing the partitioning of a Flash EEprom sector into a data area and a spare redundant area;

Fig. 6 is a circuit block diagram illustrating the data path control during read operation using the defect mapping scheme of the preferred embodiment;

Fig. 7 is a circuit block diagram illustrating the data path control during the write operation using the defect mapping scheme of the preferred embodiment;

Fig. 8 is a block diagram illustrating the write cache circuit inside the controller.

Description of the Preferred Embodiments

EEprom System

A computer system in which the various aspects of the present invention are incorporated is illustrated generally in Figure 1A. A typical computer system architecture includes a microprocessor 21 connected to a system bus 23, along with random access, main system memory 25, and at least one or more input-output devices 27, such as a keyboard, monitor, modem, and the like. Another main computer system component that is connected to a typical computer system bus 23 is a large amount of long-term, non-volatile memory 29. Typically, such a memory is a disk drive with a capacity of tens of megabytes of data storage. This data is retrieved into the system volatile memory 25 for use in current processing, and can be easily supplemented, changed or altered.

One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory, speed of access, low cost and reliability. This is accomplished by employing an array of electrically erasable programmable read only memories (EEprom's) integrated circuit chips. This type of memory has additional advantages of requiring less power to operate, and of being lighter in weight than a hard disk drive magnetic media memory, thereby being especially suited for battery operated portable computers.

The bulk storage memory 29 is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEprom integrated circuit chips. Data and instructions are communicated from the controller 31 to the EEprom array 33 primarily over a

serial data line 35. Similarly, data and status signals are communicated from the EEprom 33 to the controller 31 over serial data lines 37. Other control and status circuits between the controller 31 and the EEprom array 33 are not shown in Figure 1A.

Referring to Figure 1B, the controller 31 is preferably formed primarily on a single integrated circuit chip. It is connected to the system address and data bus 39, part of the system bus 33, as well as being connected to system control lines 41, which include interrupt, read, write and other usual computer system control lines.

The EEprom array 33 includes a number of EEprom integrated circuit chips 43, 45, 47, etc. Each includes a respective chip select and enable line 49, 51 and 53 from interface circuits 40. The interface circuits 40 also act to interface between the serial data lines 35, 37 and a circuit 55. Memory location addresses and data being written into or read from the EEprom chips 43, 45, 47, etc. are communicated from a bus 55, through logic and register circuits 57 and thence by another bus 59 to each of the memory chips 43, 45, 47 etc.

The bulk storage memory 29 of Figures 1A and 1B can be implemented on a single printed circuit card for moderate memory sizes. The various lines of the system buses 39 and 41 of Figure 1B are terminated in connecting pins of such a card for connection with the rest of the computer system through a connector. Also connected to the card and its components are various standard power supply voltages (not shown).

For large amounts of memory, that which is conveniently provided by a single array 33 may not be enough. In such a case, additional EEprom arrays can be connected to the serial data lines 35 and 37 of the controller chip 31, as indicated in Figure 1B. This is

preferably all done on a single printed circuit card but if space is not sufficient to do this, then one or more EEprom arrays may be implemented on a second printed circuit card that is physically mounted onto the first and connected to a common controller chip 31.

Erase of Memory Structures

In system designs that store data in files or blocks the data will need to be periodically updated with revised or new information. It may also be desirable to overwrite some no longer needed information, in order to accommodate additional information. In a Flash EEprom memory, the memory cells must first be erased before information is placed in them. That is, a write (or program) operation is always preceded by an erase operation.

In conventional Flash erase memory devices, the erase operation is done in one of several ways. For example, in some devices such as the Intel corporation's model 27F-256 CMOS Flash EEprom, the entire chip is erased at one time. If not all the information in the chip is to be erased, the information must first be temporarily saved, and is usually written into another memory (typically kAM). The information is then restored into the nonvolatile Flash erase memory by programming back into the device. This is very slow and requires extra memory as holding space.

In other devices such as Seeq Technology Incorporated's model 48512 Flash EEprom chip, the memory is divided into blocks (or sectors) that are each separately erasable, but only one at a time. By selecting the desired sector and going through the erase sequence the designated area is erased. While, the need for temporary memory is reduced, erase in various areas of the memory still requires a time consuming sequential

approach.

In the present invention, the Flash EEprom memory is divided into sectors where all cells within each sector are erasable together. Each sector can be addressed separately and selected for erase. One important feature is the ability to select any combination of sectors for erase together. This will allow for a much faster system erase than by doing each one independently as in prior art.

Figure 2 illustrates schematically selected multiple sectors for erase. A Flash EEprom system includes one or more Flash EEprom chips such as 201, 203, 205. They are in communication with a controller 31 through lines 209. Typically, the controller 31 is itself in communication with a microprocessor system (not shown). The memory in each Flash EEprom chip is partitioned into sectors where all memory cells within a sector are erasable together. For example, each sector may have 512 byte (i.e. 512x8 cells) available to the user, and a chip may have 1024 sectors. Each sector is individually addressable, and may be selected, such as sectors 211, 213, 215, 217 in a multiple sector erase. As illustrated in figure 2, the selected sectors may be confined to one EEprom chip or be distributed among several chips in a system. The sectors that were selected will all be erased together. This capability will allow the memory and system of the present invention to operate much faster than the prior art architectures.

Figure 3A illustrates a block diagram circuit 220 on a Flash EEprom chip (such as the chip 201 of figure 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register

such as 221, 223 associated with the respective sectors. The selection and subsequent erase operations are performed under the control of the controller 31 (see figure 2). The circuit 220 is in communication with the controller 31 through lines 209. Command information from the controller is captured in the circuit 220 by a command register 225 through a serial interface 227. It is then decoded by a command decoder 229 which outputs various control signals. Similarly, address information is captured by an address register 231 and is decoded by an address decoder 233.

For example, in order to select the sector 211 for erase, the controller sends the address of the sector 211 to the circuit 220. The address is decoded in line 235 and is used in combination with a set erase enable signal in bus 237 to set an output 239 of the register 221 to HIGH. This enables the sector 211 in a subsequent erase operation. Similarly, if the sector 213 is also desired to be erased, its associated register 223 may be set HIGH.

Figure 3B shows the structure of the register such as 221, 223 in more detail. The erase enable register 221 is a SET/RESET latch. Its set input 241 is obtained from the set erase enable signal in bus 237 gated by the address decode in line 235. Similarly, the reset input 243 is obtained from the clear erase enable signal in bus 237 gated by the address decode in line 235. In this way, when the set erase enable signal or the clear erase enable signal is issued to all the sectors, the signal is effective only on the sector that is being addressed.

After all sectors intended for erase have been selected, the controller then issues to the circuit 220, as well as all other chips in the system a global erase command in line 251 along with the high voltage for

erasing in line 209. The device will then erase all the sectors that have been selected (i.e. the sectors 211 and 213) at one time. In addition to erasing the desired sectors within a chip, the architecture of the present system permits selection of sectors across various chips for simultaneous erase.

Figures 4(1)-4(11) illustrate the algorithm used in conjunction with the circuit 220 of figure 3A. In figure 4(1), the controller will shift the address into the circuit 220 which is decoded in the line to the erase enable register associated with the sector that is to be erased. In figure 4(2), the controller shifts in a command that is decoded to a set erase enable command which is used to latch the address decode signal onto the erase enable register for the addressed sector. This tags the sector for subsequent erase. In figure 4(3), if more sectors are to be tagged, the operations described relative to figures 4(1)-4(2) are repeated until all sectors intended for erase have been tagged. After all sectors intended for erase have been tagged, the controller initiates an erase cycle as illustrated in figure 4(4).

Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Serial No. 204,175, filed June 8, 1988, by Dr. Eliyahou Harari and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," filed on the same day as the present application, by Sanjay Mehrotra and Dr. Eliyahou Harari. The disclosures of the two applications are hereby incorporate by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying

are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.

As the group of selected sectors is going through the erase cycle, some sectors will reach the "erase" state earlier than others. Another important feature of the present invention is the ability to remove those sectors that have been verified to be erased from the group of selected sectors, thereby preventing them from over-erasing.

Returning to figure 4(4), after all sectors intended for erase have been tagged, the controller initiates an erase cycle to erase the group of tagged sectors. In figure 4(5), the controller shifts in a global command called Enable Erase into each Flash EEprom chip that is to perform an erase. This is followed in figure 4(5) by the controller raising of the erase voltage line (Ve) to a specified value for a specified duration. The controller will lower this voltage at the end of the erase duration time. In figure 4(6), the controller will then do a read verify sequence on the sectors selected for erase. In figure 4(7), if none of the sectors are verified, the sequences illustrated in figures 4(5)-4(7) are repeated. In figures 4(8) and 3(9), if one or more sectors are verified to be erased, they are taken out of the sequence. Referring also to figure 3A, this is achieved by having the controller address each of the verified sectors and clear the associated erase enable registers back to a LOW with a clear enable command in bus 237. The sequences illustrated in figures 4(5)-4(10) are repeated until all the sectors in the group are verified to be erased in figure 4(11). At the completion of the

erase cycle, the controller will shift in a No Operation (NOP) command and the global Enable Erase command will be withdrawn as a protection against a false erasure.

The ability to select which sectors to erase and which ones not to, as well as which ones to stop erasing is advantageous. It will allow sectors that have erased before the slower erased sectors to be removed from the erase sequence so no further stress on the device will occur. This will increase the reliability of the system. Additional advantage is that if a sector is bad or is not used for some reason, that sector can be skipped over with no erase occurring within that sector. For example, if a sector is defective and have shorts in it, it may consume much power. A significant system advantage is gained by the present invention which allows it to be skipped on erase cycles so that it may greatly reduce the power required to erase the chip.

Another consideration in having the ability to pick the sectors to be erased within a device is the power savings to the system. The flexibility in erase configuration of the present invention enables the adaptation of the erase needs to the power capability of the system. This can be done by configuring the systems to be erased differently by software on a fixed basis between different systems. It also will allow the controller to adaptively change the amount of erasing being done by monitoring the voltage level in a system, such as a laptop computer.

An additional performance capability of the system in the present invention is the ability to issue a reset command to a Flash EEprom chip which will clear all erase enable latches and will prevent any further erase cycles from occurring. This is illustrated in figures 2A and 2B by the reset signal in the line 261.

By doing this in a global way to all the chips, less time will be taken to reset all the erase enable registers.

An additional performance capability is to have the ability to do erase operations without regard to chip select. Once an erase is started in some of the memory chips, the controller in the system can access other memory chips and do read and write operations on them. In addition, the device(s) doing the erase can be selected and have an address loaded for the next command following the erase.

Defect Mapping

Physical defects in memory devices give rise to hard errors. Data becomes corrupted whenever it is stored in the defective cells. In conventional memory devices such as RAM's and Disks, any physical defects arising from the manufacturing process are corrected at the factory. In RAM's, spare redundant memory cells on chip may be patched on, in place of the defective cells. In the traditional disk drive, the medium is imperfect and susceptible to defects. To overcome this problem manufacturers have devised various methods of operating with these defects present, the most usual being defect mapping of sectors. In a normal disk system the media is divided into cylinders and sectors. The sector being the basic unit in which data is stored. When a system is partitioned into the various sectors the sectors containing the defects are identified and are marked as bad and not to be used by the system. This is done in several ways. A defect map table is stored on a particular portion of the disk to be used by the interfacing controller. In addition, the bad sectors are marked as bad by special ID and flag markers. When the defect is addressed, the data that would normally be

stored there is placed in an alternative location. The requirement for alternative sectors makes the system assign spare sectors at some specific interval or location. This reduces the amount of memory capacity and is a performance issue in how the alternative sectors are located.

One important application of the present invention is to replace a conventional disk storage device with a system incorporating an array of Flash EEprom memory chips. The EEprom system is preferably set up to emulate a conventional disk, and may be regarded as a "solid-state disk".

In a "disk" system made from such solid-state memory devices, low cost considerations necessitate efficient handling of defects. Another important feature of the invention enables the error correction scheme to conserve as much memory as possible. Essentially, it calls for the defective cells to be remapped cell by cell rather than by throwing away the whole sector (512 bytes typically) whenever a defect occurs in it. This scheme is especially suited to the Flash EEprom medium since the majority of errors will be bit errors rather than a long stream of adjacent defects as is typical in traditional disk medium.

In both cases of the prior art RAM and magnetic disk, once the device is shipped from the factory, there is little or no provision for replacing hard errors resulting from physical defects that appear later during normal operation. Error corrections then mainly rely on schemes using error correction codes (ECC).

The nature of the Flash EEprom device predicates a higher rate of cell failure especially with increasing program/erase cycling. The hard errors that accumulate with use would eventually overwhelm the ECC and render the device unusable. One important feature

of the present invention is the ability for the system to correct for hard errors whenever they occur. Defective cells are detected by their failure to program or erase correctly. Also during read operation, defective cells are detected and located by the ECC. As soon as a defective cell is identified, the controller will apply defect mapping to replace the defective cell with a space cell located usually within the same sector. This dynamic correction of hard errors, in addition to conventional error correction schemes, significantly prolongs the life of the device.

Another feature of the present invention is an adaptive approach to error correction. Error correction code (ECC) is employed at all times to correct for soft errors as well as any hard errors that may arise. As soon as a hard error is detected, defect mapping is used to replace the defective cell with a spare cell in the same sector block. Only when the number of defective cells in a sector exceeds the defect mapping's capacity for that specific sector will the whole sector be replaced as in a conventional disk system. This scheme minimized wastage without compromising reliability.

Figure 5 illustrates the memory architecture for the cell remapping scheme. As described before, the Flash EEprom memory is organized into sectors where the cells in each sector are erasable together. The memory architecture has a typical sector 401 organized into a data portion 403 and a spare (or shadow) portion 405. The data portion 403 is memory space available to the user. The spare portion 405 is further organized into an alternative defects data area 407, a defect map area 409, a header area 411 and an ECC and others area 413. These areas contain information that could be used by the controller to handle the defects and other overhead information such as headers and ECC.

Whenever a defective cell is detected in the sector, a good cell in the alternative defects data area 407 is assigned to backup the data designated for the defective cell. Thus even if the defective cell stores the data incorrectly, an error-free copy is stored in the backup cell. The addresses of the defective cell and the backup cell are stored as defect pointers in the defect map 409.

It is to be understood that the partitioning between the user data portion 403 and the spare portion 405 need not be rigid. The relative size of the various partitioned areas may be logically reassigned. Also the grouping of the various areas is largely for the purpose of discussion and not necessarily physically so. For example, the alternative defects data area 407 has been schematically grouped under the spare portion 405 to express the point that the space it occupies is no longer available to the user.

In a read operation, the controller first reads the header, the defect map and the alternative defects data. It then reads the actual data. It keeps track of defective cells and the location of the substitute data by means of the defect map. Whenever a defective cell is encountered, the controller substitutes its bad data with the good data from the alternative defects.

Figure 6 illustrates the read data path control in the preferred embodiment. A memory device 33 which may include a plurality of Flash EEprom chips is under the control of the controller 31. The controller 31 is itself part of a microcomputer system under the control of a microprocessor (not shown). To initiate the reading of a sector, the microprocessor loads a memory address generator 503 in the controller with a memory address for starting the read operation. This information is loaded through a microprocessor interface

port 505. Then the microprocessor loads a DMA controller 507 with the starting location in buffer memory or bus address that the data read should be sent. Then the microprocessor loads the header information (Head, Cylinder and sector) into a holding register file 509. Finally, the microprocessor loads a command sequencer 511 with a read command before passing control to the controller 31.

After assuming control, the controller 31 first addresses the header of the sector and verifies that the memory is accessed at the address that the user had specified. This is achieved by the following sequence. The controller selects a memory chip (chip select) among the memory device 33 and shifts the address for the header area from the address generator 503 out to the selected memory chip in the memory device 33. The controller then switches the multiplexer 513 and shifts also the read command out to the memory device 33. Then the memory device reads the address sent it and begins sending serial data from the addressed sector back to the controller. A receiver 515 in the controller receives this data and puts it in parallel format. In one embodiment, once a byte (8 bits) is compiled, the controller compares the received data against the header data previously stored by the microprocessor in the holding register file 509. If the compare is correct, the proper location is verified and the sequence continues.

Next the controller 31 reads the defect pointers and loads these bad address locations into the holding register file 509. This is followed by the controller reading the alternative defects data that were written to replace the bad bits as they were written. The alternative bits are stored in an alternative defects data file 517 that will be accessed

as the data bits are read.

Once the Header has been determined to be a match and the defect pointers and alternative bits have been loaded, the controller begins to shift out the address of the lowest address of the desired sector to be read. The data from the sector in the memory device 33 is then shifted into the controller chip 31. The receiver 515 converts the data to a parallel format and transfers each byte into a temporary holding FIFO 519 to be shipped out of the controller.

A pipeline architecture is employed to provide efficient throughput as the data is gated through the controller from the receiver 515 to the FIFO 519. As each data bit is received from memory the controller is comparing the address of the data being sent (stored in the address generator 507) against the defect pointer map (stored in the register file 509). If the address is determined to be a bad location, by a match at the output of the comparator 521, the bad bit from the memory received by the receiver 515 is replaced by the good bit for that location. The good bit is obtained from the alternative defects data file 517. This is done by switching the multiplexer 523 to receive the good bit from the alternative defects data file instead of the bad bit from the receiver 515, as the data is sent to the FIFO 519. Once the corrected data is in the FIFO it is ready to be sent to buffer memory or system memory (not shown). The data is sent from the controller's FIFO 519 to the system memory by the controller's DMA controller 507. This controller 507 then requests and gets access to the system bus and puts out an address and gates the data via an output interface 525 out to the system bus. This is done as each byte gets loaded into the FIFO 519. As the corrected data is loaded into the FIFO it will also be

gated into an ECC hardware 527 where the data file will be acted on by the ECC.

Thus in the manner described, the data read from the memory device 33 is gated through the controller 31 to be sent to the system. This process continues until the last bit of addressed data has been transferred.

In spite of defect mapping of previously detected defective cells, new hard errors might occur since the last mapping. As the dynamic defect mapping constantly "puts away" new defective cells, the latest hard error that may arise between defect mapping would be adequately handled by the ECC. As the data is gated through the controller 31, the controller is gating the ECC bits into the ECC hardware 527 to determine if the stored value matched the just calculated remainder value. If it matches then the data transferred out to the system memory was good and the read operation was completed. However, if the ECC registers an error then a correction calculation on the data sent to system memory is performed and the corrected data re-transmitted. The method for calculating the error can be done in hardware or software by conventional methods. The ECC is also able to calculate and locate the defective cell causing the error. This may be used by the controller 31 to update the defect map associated with the sector in which the defective cell is detected. In this manner, hard errors are constantly removed from the Flash EEprom system.

Figure 7 illustrates the write data path control in the preferred embodiment. The first portion of a write sequence is similar to a read sequence described previously. The microprocessor first loads the Address pointers for the memory device 33 and the DMA as in the read sequence. It also loads the header

desired into the address generator 503 and the command queue into the command sequencer 511. The command queue is loaded with a read header command first. Thereafter, control is passed over to the controller 31. The controller then gates the address and command to the memory device 33, as in the read sequence. The memory device returns header data through controller's receiver 515. The controller compares the received header data to the expected value (stored in the holding register file 509). If the compare is correct, the proper location is verified and the sequence continues. Then the controller loads the defective address pointers from the memory device 33 into the holding register file 509 and the alternative data into the alternative defects data file 517.

Next, the controller begins to fetch the write data from system memory (not shown). It does this by getting access to the system bus, outputs the memory or bus address and does the read cycle. It pulls the data into a FIFO 601 through an input interface 603. The controller then shifts the starting sector address (lowest byte address) from the address generator 503 to the selected memory device 33. This is followed by data from the FIFO 601. These data are routed through multiplexers 605 and 513 and converted to serial format before being sent to the memory device 33. This sequence continues until all bytes for a write cycle have been loaded into the selected memory.

A pipeline architecture is employed to provide efficient throughput as the data is gated from the FIFO 601 to the selected memory 33. The data gated out of the FIFO 601 is sent to the ECC hardware 527 where a remainder value will be calculated within the ECC. In the next stage, as the data is being sent to the memory device through multiplexers 605 and 513, the comparator

521 is comparing its address from the address generator 503 to the defect pointer address values in the holding register file 509. When a match occurs, indicating that a defective location is about to be written, the controller saves this bit into the alternative defect data file 517. At the same time, all bad bits sent to memory will be sent as zeroes.

After the bytes for a write cycle have been loaded into the selected memory device, the controller issues a program command to the memory device and initiate a write cycle. Optimized implementations of write operation for Flash EEprom device have been disclosed in two previously cited co-pending U.S. patent applications, Serial No. 204,175, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques." Relevant portions of the disclosures are hereby incorporated by reference. Briefly, during the write cycle, the controller applies a pulse of programming (or writing) voltages. This is followed by a verify read to determine if all the bits have been programmed properly. If the bits did not verify, the controller repeats the program/verify cycle until all bits are correctly programmed.

If a bit fails to verify after prolonged program/verify cycling, the controller will designate that bit as defective and update the defect map accordingly. The updating is done dynamically, as soon as the defective cell is detected. Similar actions are taken in the case of failure in erase verify.

After all the bits have been programmed and verified, the controller loads the next data bits from the FIFO 601 and addresses the next location in the addressed sector. It then performs another program/verify sequence on the next set of bytes. The sequence continues until the end of the data for that

sector. Once this has occurred, the controller addresses the shadow memory (header area) associated with the sector (see figure 5) and writes the contents of the ECC registers into this area.

In addition, the collection of bits that was flagged as defective and were saved in the alternative defects data file 516 is then written in memory at the alternative defects data locations (see figure 5), thereby saving the good bit values to be used on a subsequent read. Once these data groups are written and verified, the sector write is considered completed.

The present invention also has provision for defect mapping of the whole sector, but only after the number of defective cells in the sector has exceeded the cell defect mapping's capacity for that specific sector. A count is kept of the number of defective cells in each sector. When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector. The defect pointer for the linked sectors may be stored in a sector defect map. The sector defect map may be located in the orginal defective sector if its spare area is sufficiently defect-free. However, when the data area of the sector has accumulated a large number of defects, it is quite likely that the spare area will also be full of defects.

Thus, it is preferable in another embodiment to locate the sector map in another memory maintained by the controller. The memory may be located in the controller hardware or be part of the Flash EEprom memory. When the controller is given an address to access data, the controller compares this address against the sector defect map. If a match occurs then access to the defective sector is denied and the substitute address present in the defect map is entered,

and the corresponding substitute sector is accessed instead.

In yet another embodiment, the sector remapping is performed by the microprocessor. The microprocessor looks at the incoming address and compares it against the sector defect map. If a match occurs, it does not issue the command to the controller but instead substitute the alternative location as the new command.

Apart from the much higher speed of the solid-state disk, another advantage is the lack of mechanical parts. The long seek times, rotational latency inherent in disk drives are not present. In addition, the long synchronization times, sync mark detects and write gaps are not required. Thus the overhead needed for accessing the location where data is to be read or written is much less. All of these simplifications and lack of constraints result in a much faster system with much reduced overheads. In addition, the files can be arranged in memory in any address order desired, only requiring the controller to know how to get at the data as needed.

Another feature of the invention is that defect mapping is implemented without the need to interrupt the data stream transferred to or from the sector. The data in a block which may contain errors are transferred regardless, and is corrected afterwards. Preserving the sequential addressing will result in higher speed by itself. Further, it allows the implementation of an efficient pipeline architecture in the read and write data paths.

Write Cache System

Cache memory is generally used to speed up the performance of systems having slower access devices. For example in a computer system, access of data from

disk storage is slow and the speed would be greatly improved if the data could be obtained from the much faster RAM. Typically a part of system RAM is used as a cache for temporarily holding the most recently accessed data from disk. The next time the data is needed, it may be obtained from the fast cache instead of the slow disk. The scheme works well in situations where the same data is repeatedly operated on. This is the case in most structures and programs since the computer tends to work within a small area of memory at a time in running a program. Another example of caching is the using of faster SRAM cache to speed up access of data normally stored in cheaper but slower DRAM.

Most of the conventional cache designs are read caches for speeding up reads from memory. In some cases, write caches are used for speeding up writes to memory. However in the case of writes to system memory (e.g. disks), data is still being written to system memory directly every time they occur, while being written into cache at the same time. This is done because of concern for loss of updated data files in case of power loss. If the write data is only stored in the cache memory (volatile) a loss of power will result in the new updated files being lost from cache before having the old data updated in system memory (non-volatile). The system will then be operating on the old data when these files are used in further processing. The need to write to main memory every time defeats the caching mechanism for writes. Read caching does not have this concern since the data that could be lost from cache has a backup on disk.

In the present invention, a system of Flash EEprom is used to provide non-volatile memory in place of traditional system memories such as disk storage. However, Flash EEprom memory is subject to wearing out

by excessive program/erase cycles. Even with the improved Flash EEprom memory device as disclosed in co-pending U.S. patent applications, Serial No. 204,175 and one entitled "Multi-state EEprom Read and Write Circuits and Techniques," by Sanjay Mehrotra and Dr. Eliyahou Harari filed on the same day as the present application, the endurance limit is approximately 10^6 program/erase cycles. In a ten-year projected life time of the device, this translates to a limit of one program/erase cycle per 5 minutes. This may be marginal in normal computer usage.

To overcome this problem, a cache memory is used in a novel way to insulate the Flash EEprom memory device from enduring too many program/erase cycles. The primary function of the cache is to act on writes to the Flash EEprom memory and not on reads of the Flash EEprom memory, unlike the case with traditional caches. Instead of writing to the Flash EEprom memory every time the data is updated, the data may be operated on several times in the cache before being committed to the Flash EEprom memory. This reduces the number of writes to the Flash EEprom memory. Also, by writing mostly into the faster cache memory and reducing the number of writes to the slower Flash EEprom, an additional benefit is the increase in system write throughput.

A relatively small size cache memory is quite effective to implement the present invention. This helps to overcome the problem of data loss in the volatile cache memory during a power loss. In that event, it is relatively easy to have sufficient power reserve to maintain the cache memory long enough and have the data dumped into a non-volatile memory such as a specially reserved space in the Flash EEprom memory. In the event of a power down or and power loss to the system, the write cache system may be isolated from the

system and a dedicated rechargeable power supply may be switch in only to power the cache system and the reserved space in the Flash EEprom memory.

Figure 8 illustrates schematically a cache system 701 as part of the controller, according to the present invention. On one hand the cache system 701 is connected to the Flash EEprom memory array 33. On the other hand it is connected to the microprocessor system (not shown) through a host interface 703. The cache system 701 has two memories. One is a cache memory 705 for temporarily holding write data files. The other is a tag memory 709 for storing relevant information about the data files held in the cache memory 705. A memory timing/control circuit 713 controls the writing of data files from the cache memory 705 to the Flash EEprom memory 33. The memory control circuit 713 is responsive to the information stored in the tag memory as well as a power sensing input 715 with is connected through the host interface 703 via a line 717 to the power supply of the microprocessor system. A power loss in the microprocessor system will be sensed by the memory control circuit 713 which will then down load all the data files in the volatile cache memory 705 to the non-volatile Flash EEprom memory 33.

In the present invention, the Flash EEprom memory array 33 is organized into sectors (typically 512 byte size) such that all memory cells within each sector are erasable together. Thus each sector may be considered to store a data file and a write operation on the memory array acts on one or more such files.

During read of a new sector in the Flash EEprom memory 33, the data file is read out and sent directly to the host through the controller. This file is not used to fill the cache memory 705 as is done in the traditional cache systems.

After the host system has processed the data within a file and wishes to write it back to the Flash EEprom memory 33, it accesses the cache system 701 with a write cycle request. The controller then intercepts this request and acts on the cycle.

In one embodiment of the invention, the data file is written to the cache memory 705. At the same time, two other pieces of information about the data file are written to a tag memory 709. The first is a file pointer which identifies the file present in the cache memory 705. The second is a time stamp that tells what time the file was last written into the cache memory. In this way, each time the host wishes to write to the Flash EEprom memory 33, the data file is actually first stored in the cache memory 705 along with pointers and time stamps in the tag memory 709.

In another embodiment of the invention, when a write from the host occurs, the controller first checks to see if that file already existed in the cache memory 705 or has been tagged in the tag memory 709. If it has not been tagged, the file is written to the Flash memory 33, while its identifier and time stamp are written to the tag memory 709. If the file already is present in the cache memory or has been tagged, it is updated in the cache memory and not written to the Flash memory. In this way only infrequently used data files are written into the Flash memory while frequently used data files are trapped in the cache memory.

In yet another embodiment of the invention, when a write from the host occurs, the controller first checks to see if that data file has been last written anywhere within a predetermined period of time (for example, 5 minutes). If it has not, the data file is written to the Flash memory 33, while its identifier and time stamp are written to the tag memory 709. If

the data file has been last written within the predetermined period of time, it is written into the cache memory 705 and not written to the Flash memory. At the same time, its identifier and time stamp are written to the tag memory 709 as in the other embodiments. In this way also, only infrequently used data files are written into the Flash memory while frequently used data files are trapped in the cache memory.

In all embodiments, over time the cache memory 705 will start to fill up. When the controller has detected that some predetermined state of fullness has been reached, it begins to archive preferentially some files over others in the cache memory 705 by writing them to the Flash memory 33.

In either embodiments, over time the cache memory 705 will start to fill up. When the controller has detected that some predetermined state of fullness has been reached, it begins to archive preferentially some files over others in the cache memory 705 by writing them to the Flash memory 33. The file identifier tag bits for these files are then reset, indicating that these files may be written over. This makes room for new data files entering the cache memory.

The controller is responsible for first moving the least active files back into the Flash memory 33 to make room for new active files. To keep track of each file's activity level, the time stamp for each file is incremented by the controller at every time step unless reset by a new activity of the file. The timing is provided by timers 711. At every time step (count), the controller systematically accesses each data file in the cache memory and reads the last time stamp written for this data file. The controller then increments the time stamp by another time step (i.e. increments the count by one).

Two things can happen to a file's time stamp, depending on the activity of the file. One possibility is for the time stamp to be reset in the event of a new activity occurring. The other possibility is that no new activity occurs for the file and the time stamp continues to increment until the file is removed from the cache. In practice a maximum limit may be reached if the time stamp is allowed to increase indefinitely. For example, the system may allow the time stamp to increment to a maximum period of inactivity of 5 minutes. Thus, when a data file is written in the cache memory, the time stamp for the file is set at its initial value. Then the time stamp will start to age, incrementing at every time step unless reset to its initial value again by another write update. After say, 5 minutes of inactivity, the time stamp has incremented to a maximum terminal count.

In one embodiment of keeping count, a bit can be shifted one place in a shift register each time a count increment for a file occurs. If the file is updated (a new activity has occurred) the bit's location will be reset to the initial location of the shift register. On the other hand, if the file remains inactive the bit will eventually be shifted to the terminal shift position. In another embodiment, a count value for each file is stored and incremented at each time step. After each increment, the count value is compared to a master counter, the difference being the time delay in question.

Thus, if a file is active its incremented time stamp is reset back to the initial value each time the data file is rewritten. In this manner, files that are constantly updated will have low time stamp identifiers and will be kept in cache until their activity decreases. After a period of inactivity has expired,

they acquire the maximum time stamp identifiers. The inactive files are eventually archived to the Flash memory freeing space in the cache memory for new, more active files. Space is also freed up in the tag memory when these inactive files are moved to the Flash memory.

At any time when room must be made available for new data files coming into the cache memory, the controller removes some of the older files and archives them to the Flash memory 33. Scheduling is done by a memory timing/control circuit 713 in the controller. The decision to archive the file is based on several criteria. The controller looks at the frequency of writes occurring in the system and looks at how full the cache is. If there is still room in the cache, no archiving need to be done. If more room is needed, the files with the earliest time stamps are first removed and archived to the Flash memory.

Although the invention has been described with implementation in hardware in the controller, it is to be understood that other implementations are possible. For example, the cache system may be located elsewhere in the system, or be implemented by software using the existing microprocessor system. Such variations are within the scope of protection for the present invention.

The Profile of how often data is written back to the Flash memory is determined by several factors. It depends on the size of the cache memory and the frequency of writes occurring in the system. With a small cache memory system, only the highest frequency files will be cached. Less frequently accessed files will also be cached with increasing cache memory size. In the present invention, a relatively cheap and small amount of cache memory, preferably about 1 Mbyte, may be used to good advantage. By not constantly writing the

most active files (the top 5%), the write frequency of the Flash EEprom may be reduced from the usual one every millisecond to one every 5 minutes. In this way the wear-out time for the memory can be extended almost indefinitely. This improvement is also accompanied by increased system performance during write.

Incorporating time tag into the write cache concept has the advantage that the size of the write cache buffer memory can be relatively small, since it is used only to store frequently written data files, with all other files written directly into the Flash EEprom memory. A second advantage is that the management of moving data files in and out of the write cache buffer can be automated since it does not require advanced knowledge of which data files are to be called next.

The various aspects of the present invention that have been described co-operate in a system of Flash EEprom memory array to make the Flash EEprom memory a viable alternative to conventional non-volatile mass storage devices.

While the embodiments of the various aspects of the present invention that have been described are the preferred implementation, those skilled in the art will understand that variations thereof may also be possible. Therefore, the invention is entitled to protection within the full scope of the appended claims.

IN THE CLAIMS:

1. A Flash EEprom system comprising:

one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously;

means for selecting a plurality of sectors among the one or more chips for erase operation; and

means for simultaneously performing the erase operation on only the plurality of selected sectors.

2. A Flash EEprom system as in claim 1, including

read or write operations on chips which have been enabled by a chip select signal, wherein the erase operation is performed on chips without regard to the chip select signal.

3. A Flash EEprom system as in claim 1, wherein the erase operation may be performed on the plurality of sector selected for erase operation, while read, write or other operations may be performed on any other device not selected for erase operation.

4. The Flash EEprom system according to claim 1, further comprising:

means for individually removing any one or combination of sectors from the plurality of selected sectors, such that said removed sectors are prevented from further erase during the erase operation.

5. The Flash EEprom system according to claim 1, further comprising:

means for simultaneously deselecting all sectors.

6. The Flash EEprom system according to claim 1, wherein the selecting means further comprises:

individual register associated with each sector for holding a status to indicate whether the sector is selected or not.

7. The Flash EEprom system according to claim 6, wherein the simultaneously erasing means is responsive to the status in each of the individual registers, such that only the selected sectors are included in the erasing.

8. The Flash EEprom system according to claim 6, wherein any one or combination of the individual registers indicating a selected status are individually resettable to an un-selected status.

9. The Flash EEprom system according to claim 6, wherein all the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected.

10. A system for correcting errors from defective cells within an array of Flash EEprom cells, comprising:

substitute cells;

means for substituting one or more of the defective cells with a corresponding number of substitute cells.

11. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 10 wherein the substituting means also applies automatically to new defective cells as soon as they are detected.

12. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 10, said array being partitioned into a plurality of Flash erasable sectors such that all cells within each sector are erasable at once, wherein the substitute cells are in the same sector as the defective cells.

13. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 11, further comprising a defect map for storing defect pointers which link the addresses of the defective cells to that of the corresponding substitute cells.

14. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 13, wherein the defect map for said defective cells are located in the same sector as said defective cells.

15. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 10, said array being partitioned into a plurality of Flash erasable sectors such that all cells within each sector are erasable at once, wherein the substitute cells are in the same sector as the defective cells when the number of defective cells in the sector does not exceed a predetermined number, and the substitute cells are in a different sector when the number is exceeded.

16. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 15, wherein said sector is replaced in its entirety by a substitute sector when said number is exceeded.

17. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 15 wherein the substituting means also applies automatically new defective cells as soon as they are detected.

18. A system for correcting errors from defective cells within an array of Flash EEprom cells as in claim 17, including the use of error correction codes.

19. A system for correcting bad data in defective cells within an array of Flash EEprom cells, comprising:

substitute cells for storing good data intended for the defective cells;

means for substituting the bad data in one or more of the defective cells with the good data in the corresponding substitute cells when the defective cells are accessed.

20. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 19, further comprising means for automatically saving the good data intended to be written to the defective cells to the corresponding substitute cells, thereby perserving the integrity of the good data.

21. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 20 wherein the substituting means also applies automatically to new defective cells as soon as they are detected.

22. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 20, said array being partitioned into a plurality of Flash erasable sectors such that all cells within each sector are erasable at once, and data is stored therein, wherein the substituting means applies after the data including the bad data has been accessed.

23. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 20, said array being partitioned into a plurality of Flash erasable sectors such that all cells within each sector are erasable at once, wherein the substitute cells are in the same sector as the defective cells.

24. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 20, further comprising a defect map for storing defect pointers which link the addresses of the defective cells to that of the corresponding substitute cells.

25. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 24, wherein the defect map for said defective cells are located in the same sector as said defective cells.

26. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 19, said array being partitioned into a plurality of Flash erasable sectors such that all cells within each sector are erasable at once, wherein the substitute cells are in the same sector as the defective cells when the number of defective cells in the sector does not exceed a predetermined number, and the substitute cells are in a different sector when the number is exceeded.

27. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 26, wherein said sector is replaced in its entirety by a substitute sector when said number is exceeded.

28. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 26, wherein the substituting means also applies automatically to newly occurring defective cells.

29. A system for correcting bad data in defective cells within an array of Flash EEprom cells as in claim 28, including use of error correction codes.

30. An improved system for writing data files into a Flash EEprom memory comprising:

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

means responsive to a system write to the Flash EEprom memory for writing data files into the cache memory instead of the Flash EEprom memory;

means for identifying each data file in the cache memory;

means for determining the time since each data file was last written; and

means for first moving data file having the longest time since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

31. The improved system as in claim 30, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

means responsive to an impending power loss for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

32. The improved system as in claim 30, wherein the backup memory is part of the Flash EEprom memory.

33. The improved system as in claim 30, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

34. The improved system as in claim 30, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

35. The improved system as in claim 30, including a microprocessor system and random access memory, wherein the improved system is implemented by software in the microprocessor system with random access memory.

36. An improved system for writing data files into a Flash EEprom memory comprising:

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

means responsive to a system write to the Flash EEprom memory for writing data files into the cache memory instead of the Flash EEprom memory;

a tag memory for storing the identity of data files and the time each data file was last written; and

means for first moving data file having the longest time since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

37. The improved system as in claim 36, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

means responsive to an impending power loss for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

38. The improved system as in claim 36, wherein the backup memory is part of the Flash EEprom memory.

39. The improved system as in claim 36, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

40. The improved system as in claim 36, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

41. The improved system as in claim 36, including a microprocessor system and random access memory, wherein the improved system is implemented by software in the microprocessor system with random access memory.

42. An improved system for writing data files into a Flash EEprom memory comprising:

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

means responsive to a system write to the Flash EEprom memory for writing a data file either into the Flash EEprom memory or instead into the cache memory, said responsive means writing to the Flash EEprom when the a previous copy of said data file is not present in the cache memory, and writing to the cache memory when a previous copy of said data file is present in the cache memory; and

means for first moving data files having the longest times since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

43. The improved system as in claim 42, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

means responsive to an impending power loss for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

44. The improved system as in claim 42, wherein the backup memory is part of the Flash EEprom memory.

45. The improved system for writing data files into a Flash EEprom memory according to claim 42, wherein said responsive means for writing includes a tag memory for storing the identity of data files and the time each data file was last written, and wherein said responsive means writing to the Flash EEprom when said data file is not tagged in the tag memory, and writing to the cache memory when said data file is tagged in the tag memory.

46. An improved system for writing data files into a Flash EEprom memory comprising:

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

means responsive to a system write to the Flash EEprom memory for writing a data file either into the Flash EEprom memory or instead into the cache memory, said responsive means writing to the Flash EEprom when said data file is last written after the predetermined period of time, and writing to the cache memory when said data file is last written within a predetermined period of time; and

means for first moving data files having the longest times since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

47. The improved system as in claim 46, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

48. The improved system as in claim 46, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

49. The improved system as in claim 46, including a microprocessor system and random access memory, wherein the improved system is implemented by software in the microprocessor system with random access memory.

50. An improved system for writing data files into a Flash EEprom memory comprising:

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

a tag memory for storing the identity of data files and the time each data file was last written;

means responsive to a system write to the Flash EEprom memory for writing a data file either into the Flash EEprom memory or instead into the cache memory, said responsive means writing to the Flash EEprom when the data file is not identified in the tag memory, and writing to the cache memory when the data file is identified in the tag memory; and

means for moving first the data files having the longest times since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

51. The improved system as in claim 50, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

means responsive to an impending power loss for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

52. The improved system as in claim 50, wherein the backup memory is part of the Flash EEprom memory.

53. The improved system as in claim 50, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

54. The improved system as in claim 50, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

55. The improved system as in claim 50, including a microprocessor system and random access memory, wherein the improved system is implemented by software in the microprocessor system with random access memory.

56. A memory card adapted to plug into a computer system in a manner to communicate with a system bus and a standard power supply, comprising the following mounted thereon:

a plurality of EEprom integrated circuit chips, each of said chips including:

a large number of individually addressable storage cells organized into a plurality of sectors, each sector containing a plurality of said storage cells,

a plurality of spare storage cells within any of said sectors,

means responsive to signals on said system bus for erasing all cells in one or more designated sectors without erasing cells in others of said sectors,

means responsive to signals on said system bus for reading the state of addressed storage cells,

means responsive to signals on said system bus for programming addressed storage cells to a predetermined state, and

means responsive to an unsuccessful attempt to either program or erase a storage cell within one of said sectors for substituting one of said spare storage cells therefore while maintaining operation of the remaining cells of said sector.

57. The memory card according to claim 56 which additionally comprises a cache memory mounted on said card, and wherein said programming means includes means for initially programming said cache memory rather than said EEprom memory, said reading means includes means for initially determining whether the cache memory contains data to be read, and said programming means additionally includes means responsive to said cache memory becoming full for writing its oldest unused block of data into said EEprom memory, thereby to make room for new data in said cache memory.

58. The memory card as in claim 56, wherein each of said chips further includes a plurality of spare sectors, and wherein said substituting means also substitutes one of said spare sectors for one of said sectors when a predetermined number of cells in said one of said sector become defective.

59. The memory card as in claim 58, including means for performing error correction using error correction codes.

60. The memory card as in claim 56, including a controller and an interface connected to the system bus, said controller being adapted to be responsive to commands intended for a standard magnetic disk drive storage system connectable to the computer system, thereby emulating said disk drive system.

61. The memory card as in claim 56, in which various operating voltages are required for various operations of the EEprom chips, including means for generating the various operating voltages from the standard power supply.

62. A storage system incorporating therein the memory card of claim 56, comprising:

a controller for controlling the operation of the EEprom chips;

means for generating voltages for the operation of the EEprom chips;

means for error correction in the operation of the storage system; and

means for interfacing the storage system to a computer system.

08/174,768

ABSTRACT

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

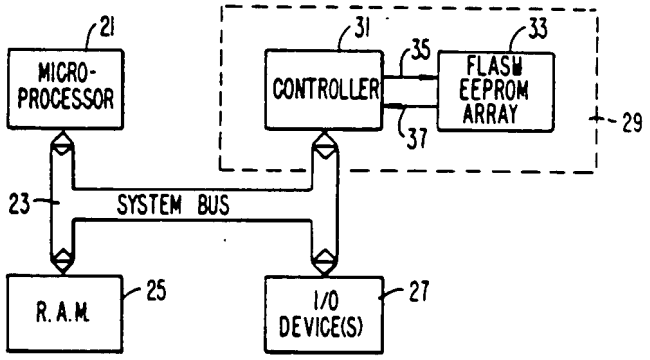


FIG._1A.

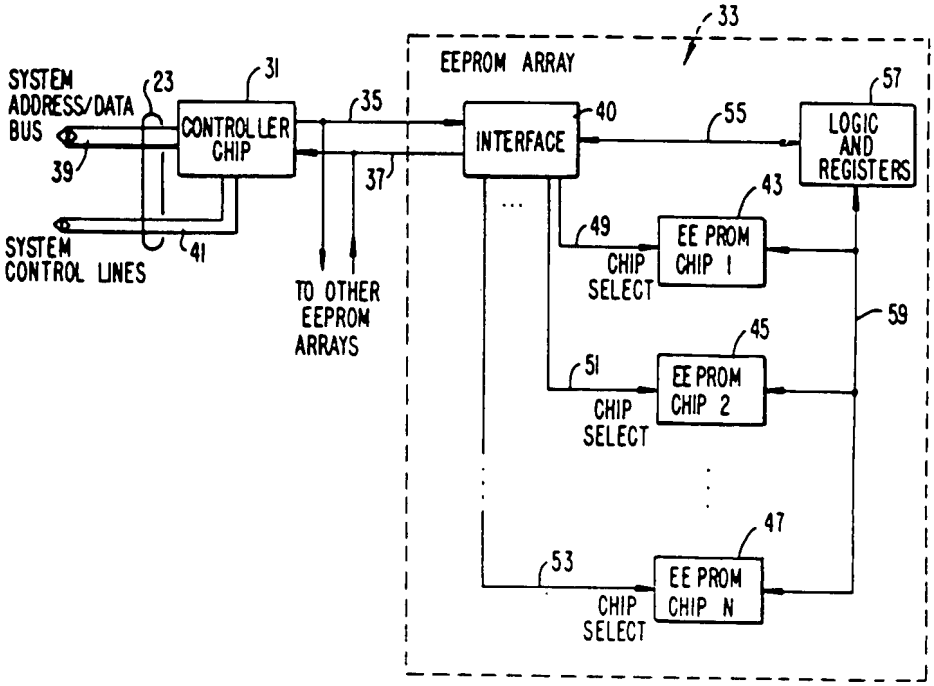


FIG._1B.

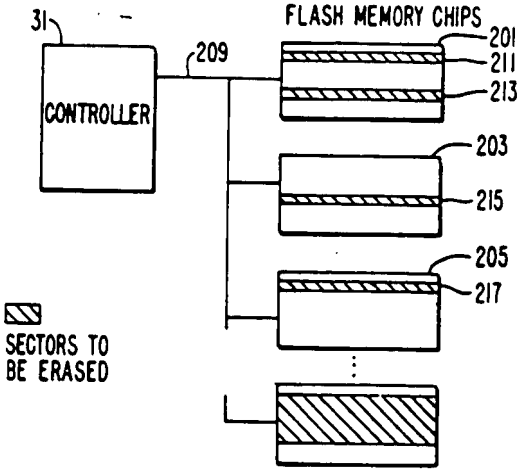


FIG._2.

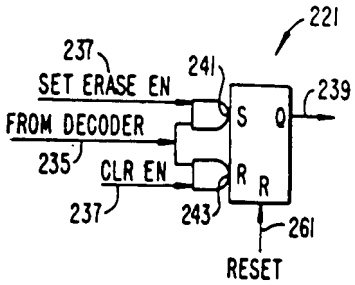


FIG._3B.

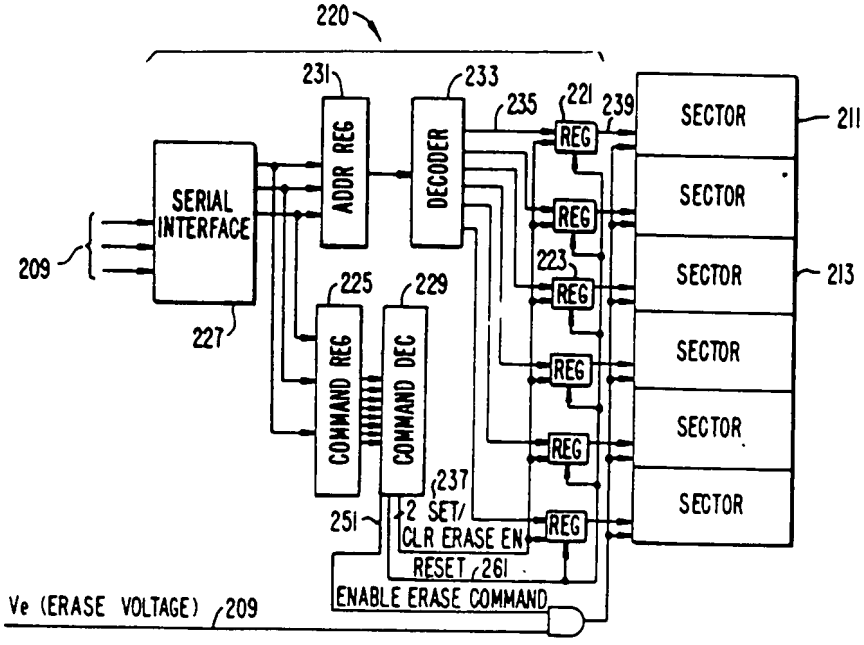


FIG._3A.

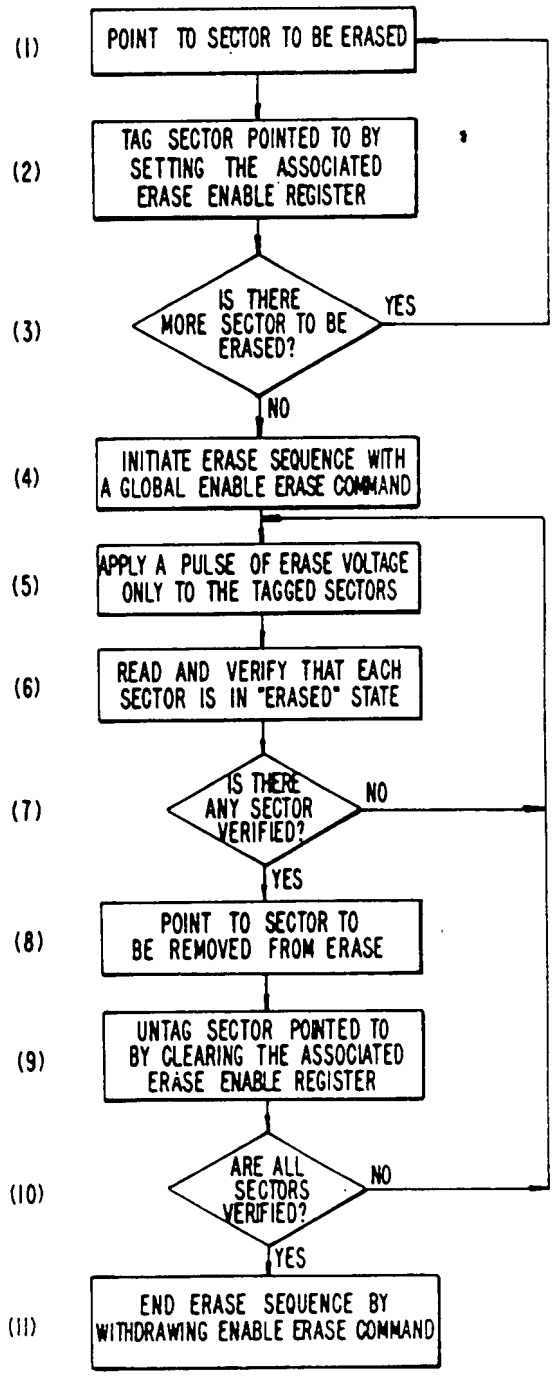
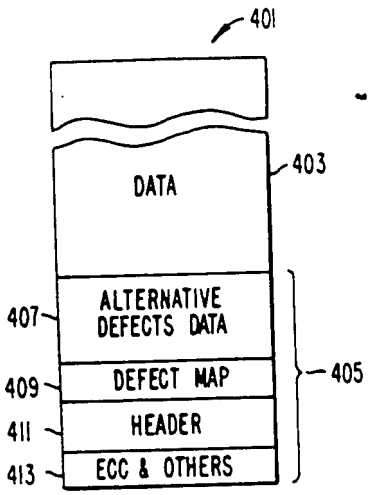


FIG._4.



SECTOR PARTITION

FIG._5.

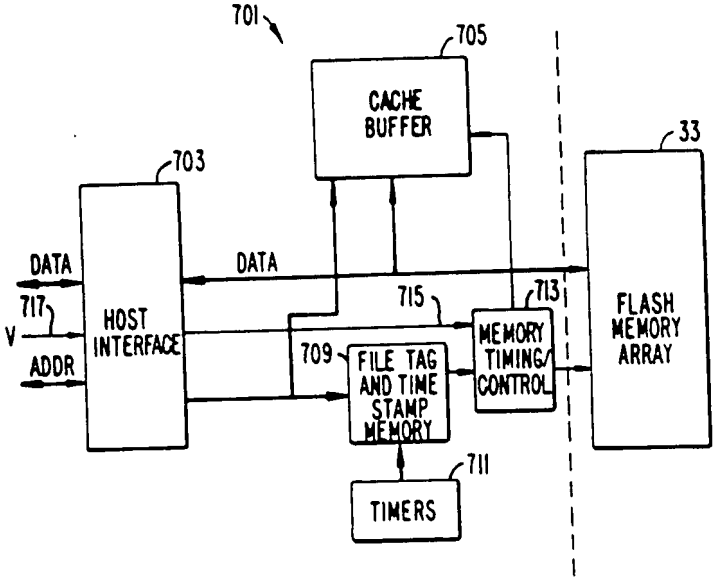
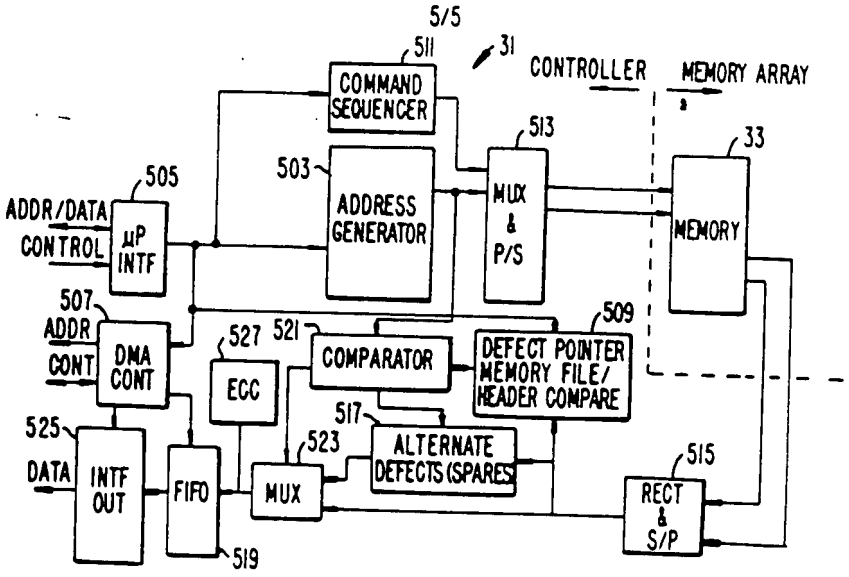
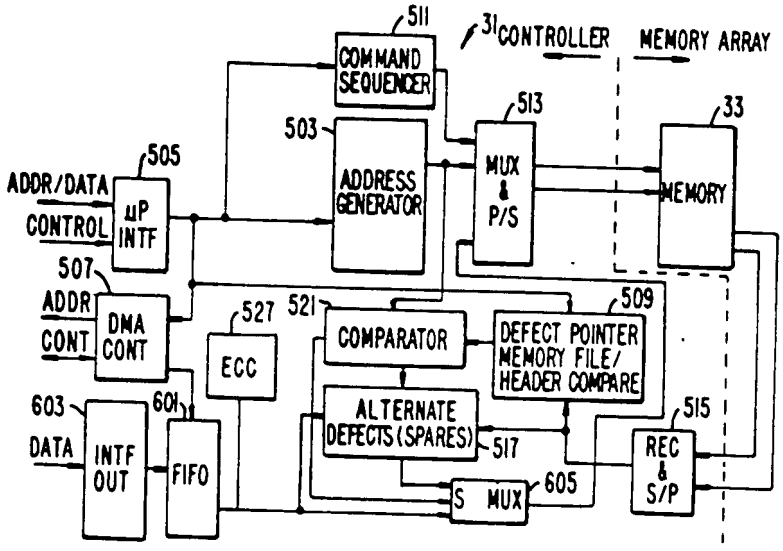


FIG._8.



READ DATA PATH CONTROL

FIG._6.



WRITE DATA PATH CONTROL

FIG._7.

#1

PATENT APPLICATION DECLARATION

(Attorney's Docket No.: HARI-0600)

Each of the Applicants named below hereby declares as follows:

1. My residence, post office address and country of citizenship given below are true and correct.

2. I believe I am the original, first and joint inventor of the invention claimed in the patent application specification Serial No. 337,566, filed April 13, 1989, for which a patent is sought, and I have reviewed and understand the contents of the attached specification, including its claims.

3. I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application. I understand that information is material where there is a substantial likelihood that a reasonable patent examiner would consider it important in deciding whether to allow the attached application to issue as a patent.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Additionally, the undersigned hereby appoint the following as attorneys and agents to prosecute said patent application, to transact all business in the Patent and Trademark Office connected therewith, to receive the original Letters Patent and to substitute or associate other attorneys on my behalf:

Gerald P. Parsons	Registration No. 24,486
Martin F. Majestic	Registration No. 25,695
J. Suzanne Siebert	Registration No. 26,758
James S. Hsue	Registration No. 29,545
Philip Yau	Registration No. 32,892

Please send all correspondence to:

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Date: 5.15, 1989

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Date: 5.16, 1989

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Date: 5.15., 1989

Sanjay Mehrotra

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735 Berkshire Place
Milpitas, CA 95035
(Citizenship: India)

BAR CODE LABEL

U.S. PATENT APPLICATION

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT
08/174,768	12/29/93 RULE 60	371	2313

APPLICANT

ELIYAHOU HARARI, LOS GATOS, CA; ROBERT D. NORMAN, SAN JOSE, CA; SANJAY MEHROTRA, MILPITAS, CA.

CONTINUING DATA********
VERIFIED THIS APPLN IS A CON OF 07/963,838 10/20/92 PAT 5,297,148
AND A DIV OF 07/337,566 04/13/89 ABN

FOREIGN/PCT APPLICATIONS********
VERIFIED

FOREIGN FILING LICENSE GRANTED 02/09/94

STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS	FILING FEE RECEIVED	ATTORNEY DOCKET NO.
CA	5	7	1	$710.00	HARI0606

ADDRESS

GERALD P. PARSONS
MAJESTIC, PARSONS, SIEBERT & HSUE
FOUR EMBARCADERO CENTER, SUITE 1450
SAN FRANCISCO, CA 94111-4121

TITLE

FLASH EEPROM SYSTEM

This is to certify that annexed hereto is a true copy from the records of the United States Patent and Trademark Office of the application which is identified above.

By authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

Date

Certifying Officer

PATENT APPLICATION SERIAL NO. 08/174768

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

09.

PTO-1556
(5/87)

PTO 1130 (REV 11/91)

U.S. DEPARTMENT OF COMMERCE- PATENT & TRADEMARK OFFICE

PACE DATA ENTRY CODING SHEET

1ST EXAMINER [illegible] DATE 2-7-94

2ND EXAMINER DATE

APPLICATION NUMBER	TYPE APPL	FILING DATE MONTH	DAY	YEAR	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWING
08/174768	1	12	29	93	2	2313	377	5

TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE	FOREIGN LICENSE	ATTORNEY DOCKET NUMBER
17	1	0	710	Y	HARI0606

CONTINUITY DATA

CONTINUITY CODE	STATUS CODE	PARENT APPPLICATION SERIAL NUMBER	PARENT PATENT NUMBER	PARENT FILING DATE MONTH	DAY	YEAR
02	2	07/963,838		10	20	92
01	3	07/337,566		04	13	89

PCT/FOREIGN APPLICATION DATA

FOREIGN PRIORITY CLAIMED	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FOREIGN FILING DATE MONTH	DAY	YEAR

SAN0000761

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1992

Application or Docket Number: 17476P

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
FOR							
BASIC FEE				$355.00	OR		$710.00
TOTAL CLAIMS	7 minus 20 =	*	x$11=		OR	x$22=	
INDEPENDENT CLAIMS	1 minus 3 =	*	x 37=		OR	x 74=	
MULTIPLE DEPENDENT CLAIM PRESENT			+115=		OR	+230=	
			TOTAL		OR	TOTAL	711

* If the difference in column 1 is less then zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
AMENDMENT A	Total	* 13	Minus	**	=	x$11=		OR	x$22=	
	Independent	* 2	Minus	***	=	x 37=		OR	x 74=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+ 115=		OR	+230=	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	
AMENDMENT B	Total	* 35	Minus	** 20	= 15	x$11=		OR	x$22=	330
	Independent	* 5	Minus	*** 3	= 2	x 37=		OR	x 74=	158
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						TOTAL ADDIT FEE		OR	TOTAL ADDIT. FEE	488
AMENDMENT C	Total	* 81	Minus	** 35	= 46	x$11=		OR	x$22=	1012
	Independent	* 5	Minus	*** 5	=	x 37=		OR	x 74=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				*	+115=		OR	~~+230=~~	240
						TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	1252

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20"

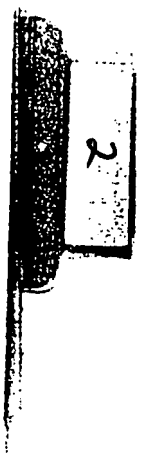
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3"

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1

FORM PTO-875 (Rev. 10-92)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

SAN000762


2

11

08/174768

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
)
ELIYAHOU HARARI, ROBERT D.)
NORMAN and SANJAY MEHROTRA)
)
For: FLASH EEPROM SYSTEM)
)

PARENT APPLICATION
ASSIGNED TO GROUP
ART UNIT 2313

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING UNDER 37 CFR 1.10

I hereby certify that this patent application transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" Mailing Label Number TB32760177X addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on December 29, 1993.

Name: Brenda J. Dolly

Signature 12/29/93 Date

CONTINUATION APPLICATION TRANSMITTAL

Sir:

This is a request for filing a continuation application under 37 CFR 1.60 of pending prior application Serial No. 07/963,838, filed October 20, 1992, by Eliyahou Harari, Robert D. Norman and Sanjay Mehrotra, for FLASH EEprom SYSTEM.

1. Enclosed is a copy of the prior application, including the Declaration of the inventors as originally filed. I hereby certify that the attached papers are a true copy of prior application Serial No. 07/963,838 as originally filed on October 20, 1992, as appears in the files of the undersigned attorney, and that no amendments referred to in the oath or declaration (if any) filed to complete the prior application introduced new matter therein.

2. Cancel in this application original claims 1-55 of the prior application before the filing fee is calculated.

3. The filing fee is calculated to be $710.00, a check for which is enclosed. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

4. Amend the specification by inserting on page one, before the line 4, the following new section:

Cross-Reference to Related Applications

This application is a continuation of co-pending application Serial No. 07/963,838, filed October 20, 1992, now patent no. 5,297,148, which in turn is a division of original application Serial No. 07/337,566, filed April 13, 1989, now abandoned, which are hereby incorporated herein by this reference.

~~The following related patents and patent applications are~~ also incorporated herein by this reference:

Patent No. 5,095,344	3/10/92	Highly Compact EPROM and Flash EEPROM Devices
Patent No. 5,172,338	12/15/92	Multi-State EEPROM Read and Write Circuits and Techniques
Patent No. 5,200,959	04/06/93	Device and Method for Defect Handling in Semi-Conductor Memory
Patent No. 5,270,979	12/14/93	Method for Optimizing Erasing of EEPROM
Serial No. 07/919,715	07/24/92	Segmented Column Memory Array
Serial No. 07/629,250	12/18/90	Dense Vertical Read Only Memory Cell Structures and Processes for Making Them
Serial No. 08/148,932	11/08/93	Streamlined ~~Write~~ Operation For EEPROM System
Serial No. 08/148,930	11/08/93	Mixed Data Encoding EEPROM System
Serial No. 08/149,602	11/08/93	Method for Optimizing Erasing of EEPROM
Serial No. 07/948,175	09/21/92	Latent Defect Handling in EEPROM Devices
Serial No. 07/736,733	07/26/91	Device and Method for Controlling Solid-State Memory System

Serial No. 07/736,732	07/26/91	Computer Memory Cards Using Flash EEPROM Integrated Circuit Chips and Memory-Controller Systems
Serial No. 07/759,212	09/13/91	Wear Leveling Techniques for Flash EEPROM Systems
Serial No. 07/759,497	09/13/91	Flash EEPROM Array Data and Header File Structure
Serial No. 07/886,080	05/20/92	Soft Errors Handling in EEPROM Devices
Serial No. 08/151,292	11/12/93	Removable Mother/Daughter ~~Peripheral Card~~

5. The prior application is assigned of record to SunDisk Corporation.

6. Five (5) sheets of formal drawings are also enclosed.

7. The Power of Attorney appearing in the prior application is to Gerald P. Parsons (Reg. No. 24,486), Martin F. Majestic (Reg. No. 25,695), J. Suzanne Siebert (Reg. No. 28,758), and James S. Hsue (Reg. No. 29,545), and Philip Yau (Reg. No. 32,892).

8. Address all future communications to:

Gerald P. Parsons, Esq.
MAJESTIC, PARSONS, SIEBERT & HSUE
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Telephone: (415) 362-5556
Facsimile: (415) 362-5418

Dated: December 29, 1993

Gerald P. Parsons, Reg. No. 24,486
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San Francisco, CA 94111-4121

Docket No.: HARI-0606


3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
ELIYAHOU HARARI, *et al.*)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2313

#3

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING UNDER 37 CFR 1.10

I hereby certify that this patent application transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" Mailing Label Number TB614039217US addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on December 22, 1994.

Julie M. Barot

Signature Date

DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Disclosure Statement submitted for the Examiner's consideration. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, are respectfully requested.

Respectfully submitted,

Dated: December 22, 1994

Gerald P. Parsons

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Telephone: (415) 362-5556
Facsimile: (415) 362-5418
Attorney for Applicant

GPP:jmb
Atty. Docket: HARI-0606

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI-0606	08/174,768
		APPLICANT: ELIYAHOU HARARI, et al.	
	INFORMATION DISCLOSURE ACTION (Use several sheets if necessary)	FILED: December 29, 1993	GROUP: 2313

MAIL ROOM 36 22 1994 PAT. & TRADEMARK OFF.

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
[illegible]	A1	4 2 8 1 3 9 8	7/28/81	McKenny, et al.	365	200	
[illegible]	A2	4 6 1 7 6 5 1	10/14/86	Ip, et al.	365	200	
[illegible]	A3	5 0 4 3 9 4 0	8/27/91	Harari	365	185.03	
[illegible]	A4	5 2 9 7 1 4 8	3/22/94	Harari, et al.	365	207	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

EXAMINER	DATE CONSIDERED
Ly V. Hua	4/7/95

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of
ELIYAHOU HARARI, *et al.*
Serial No.: 08/174,768
Filed: December 29, 1993
For: FLASH EEPROM SYSTEM

Group Art Unit: 2313

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING UNDER 37 CFR 1.10

I hereby certify that this patent application transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" Mailing Label Number TB614039217US addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on December 22, 1994.

Julie M. Balot
Signature
Date

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent application, prior to a first Examiner's Action, by cancelling claims 56-62, all of the claims now in the application, and substitute the following new claims therefore:

~~56~~63. A memory system on a card that is connectable to a computer system, comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit,

means including a memory controller that is connectable

to said computer system for controlling operation of the array,

means for linking any defective ones of said plurality of sectors to others of said sectors, and

means for accessing linked others of said sectors in place of said defective sectors.--

--64. The memory system card of claim 63 wherein said linking means is stored in the array.--

--65. The memory system card of claim 63 wherein said accessing means is within the controller.--

--66. The memory system card of claim 63 wherein said accessing means is within a processor of the computer system.--

--67. The memory system card of claim 63 wherein said memory card is characterized by being compatible with a magnetic disk drive storage system and capable of substituting therefor in said computer system.--

--68. The memory system card of claim 63 wherein said sector linking means includes a list of defect pointers which map defective sectors into one of the others of said sectors.--

--69. The memory system card of claim 68 which additionally comprises means responsive to a number of defective cells within a particular sector exceeding a certain number for adding a defect pointer to said list for mapping said particular sector into another sector.--

--70. A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, and a controller connectable to said processor for controlling operation of the array, comprising:

identifying when a sector becomes defective,

storing an address of the defective sector in a sector defect map,

linking with the defective sector address in the defect map an address of another sector that is not defective, and

accessing a sector of the memory system by, when the sector being accessed is defective, referring to the sector defect map to translate the address of the defective sector being accessed into an address of another sector that is not defective, thereby to remap the defective sector into another sector that is ~~not defective~~.--

--71. The method of claim 70 wherein accessing a sector of the memory includes first comparing an address of the desired sector with the addresses of defective sectors that are stored in the sector defect map, and then either, (a) if the desired sector address is not stored in the sector defect map, accessing the sector which has the desired address, thereby leaving the sector addressing undisturbed by the sector defect map, or (b) if the desired sector address is stored in the sector defect map, accessing the sector that is not defective whose address is linked therewith in the sector defect map.--

--72. The method of claim 70 wherein the sector defect map is stored in the memory cell array.--

--73. The method of claim 70 wherein accessing a sector of the memory is performed by the controller.--

--74. The method of claim 70 wherein accessing a sector of the memory is performed by the processor.--

--75. The method of claim 70 wherein identifying when a sector becomes defective includes identifying when a sector has a number of defective memory cells therein which exceeds a given number.--

REMARKS

This Amendment is being filed prior to an Examiner's Action in the present continuation application, in order to substitute a new set of claims for those originally filed. These claims are directed to the feature of defective sector substitution that is described on pages 23 and 24, and elsewhere, of the present application specification.

An Information Disclosure Statement, and copies of the

references listed therein, are also being filed herewith.

An early examination and allowance of the present application, as amended, is solicited.

Respectfully submitted,

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Attorney for Applicant

GPP:jmb
Atty. Docket: HARI-0606

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Yanou Harari et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2313

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on January 5, 1995.

Lois Simon Petitpas

Lois Simon Petitpas
Signature

Date 1/5/95

SUPPLEMENTAL DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Supplemental Disclosure Statement to the Disclosure Statement filed December 22, 1994, submitted for the Examiner's consideration. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, are respectfully requested.

Dated: January 5, 1995

Respectfully submitted,

Gerald P. Parsons

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Atty. Docket: HARI-0606

Sheet 1 of 1

FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI-0606	08/174,768
INFORMATION DISCLOSURE ACTION *(Use several sheets if necessary)*		APPLICANT Eliyahou Harari et al.	
		FILED December 29, 1993	GROUP 2313

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
EH	1	4 4 9 3 0 7 5	1/8/85	Anderson et al.	365	200	
EH	2	4 7 9 6 2 3 3	1/3/89	Awaya et al.	365	200	
EH	3	4 9 1 4 5 2 9	4/3/90	Bonke	360	48	
EH	4	4 0 5 1 3 5 4	9/27/77	Choate	365	200	
EH	5	4 7 5 7 4 7 4	7/12/88	Fukushi et al.	365	187.07	
EH	6	4 7 3 3 3 9 4	3/22/88	Giebel	365	235.01	
EH	7	4 5 1 4 8 3 0	4/30/85	Hagiwara et al.	365	155.05	
EH	8	4 7 9 4 5 6 8	12/27/88	Lim et al.	365	185.18	
EH	9	4 6 1 2 6 4 0	9/16/86	Mehrotra et al.	371	40.01	
EH	10	4 5 2 7 2 5 1	7/2/85	Nibby, Jr. et al.	375	182.08	
EH	11	4 7 4 6 9 9 8	5/24/88	Robinson et al.	360	72.1	
EH	12	4 9 4 2 5 5 6	7/17/90	Sasaki et al.	365	200	
EH	13	4 7 7 4 7 0 0	9/27/88	Satoh et al.	307	57	
EH	14	4 4 0 5 9 5 2	9/20/83	Slakmon	360	47	
EH	15	4 6 7 2 2 4 0	6/9/87	Smith et al.	321	15	
EH	16	4 6 8 8 2 1 9	8/18/87	Takemae	365	240	
EH	17	4 2 5 0 5 7 0	2/10/81	Tsang et al.	365	200	
EH	18	4 6 0 1 0 3 1	7/15/86	Walker et al.	371	30X	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

EXAMINER	DATE CONSIDERED
Ly V Hua	4/7/95

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Eliyahou Harari et al.

Serial No.: 08/174,768

Filed: December 29, 1993

For: FLASH EEPROM SYSTEM

Group Art Unit: 2313

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on January 12, 1995.

Lois Simon Petitpas

Lois Simon Petitpas 1/12/95

Signature Date

SECOND SUPPLEMENTAL DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Second Supplemental Disclosure Statement to the Supplemental Disclosure Statement filed on January 5, 1995 and the Disclosure Statement filed December 22, 1994, submitted for the Examiner's consideration. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, are respectfully requested.

Dated: January 12, 1995

Respectfully submitted,

Gerald P. Parsons

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Atty. Docket: HARI-0606

Part 7 Paper #6

Sheet 1 of 1

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI-0606	08/174,768
INFORMATION DISCLOSURE ACTION (Use several sheets if necessary)		APPLICANT: Eliyahou Harari	
		FILED: December 29, 1993	GROUP: 2313

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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
EH	1	4 3 5 5 3 7 6	10/19/82	Gould	365	200	
EH	2	3 6 3 3 1 7 5	1/4/72	Harper	395	435	
EH	3	4 4 9 8 1 4 6	2/5/85	Martinez	395	442	
EH	4	4 9 2 4 3 3 1	5/8/90	Robinson et al.	360	72.1	
EH	5	4 4 7 9 2 1 4	10/23/84	Ryan	371	2.2	
EH	6	4 9 5 3 1 2 2	8/28/90	Williams	395	104	
EH	7	4 9 4 9 3 0 9	8/14/90	Rao	365	185.12	
EH	8	4 9 2 0 5 1 8	4/24/90	Nakamura et al.	365	228	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

EXAMINER	DATE CONSIDERED
	4/10/95

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

146.-103

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#7/C

In re Patent Application of)
ELIYAHOU HARARI, *et al.*) Group Art Unit: 2313
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

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3/7/95

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

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HUA:-

CERTIFICATE OF EXPRESS MAILING UNDER 37 CFR 1.10

I hereby certify that this patent application transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" Mailing Label Number TB614037633 addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on February 10, 1995.

Brenda J. Dolly

Brenda J. Dolly 2/10/95
Signature Date

SECOND PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent application, prior to a first Examiner's Action, as follows:

P 30134 03/09/95 08174768 13-1030 039 103 158.00CR

IN THE SPECIFICATION:

In the section entitled "Cross-Reference to Related Applications" which was added to page one of the present application by the Continuation Application Transmittal filed with the application on December 29, 1993, please change the following:

Line 3, replace "_,___,___" with --5,297,148--; and

Cancel the entire second paragraph, including the list of related patents and applications, beginning with "The Following.." and extending through "..Peripheral Card".

Serial No.: 08/174,768

158.00 dlc

IN THE CLAIMS:

Amend claim 70, as follows:

70. (Amended) A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, [and a controller connectable to said processor for controlling operation of the array,] comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

identifying when a sector becomes defective,

storing an address of the defective sector in a sector defect map,

linking with the defective sector address in the defect map an address of another sector that is not defective, and

accessing a sector of the memory system by, when the sector being accessed is defective, referring to the sector defect map to translate the address of the defective sector being accessed into an address of another sector that is not defective, thereby to remap the defective sector into another sector that is not ~~defective.~~

Add the following new claims:

--76. The method according to claim 70, additionally comprising storing in individual ones of said sectors both user data and overhead information related to either the accessed usable sector or the user data stored therein.--

--77. The method according to claim 76, wherein the storing of overhead information includes storing sector addresses in the individual sectors that are related to the addresses of the individual sectors in which they are stored.--

--78. The method according to claim 76, wherein the storing of overhead information includes storing in the individual sectors error correction codes for user data stored in ~~corresponding individual sectors.~~--

--79. A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

detecting a predefined condition when individual sectors become unusable and adding addresses of such unusable sectors to a list maintained within the card that links such unusable sector addresses with addresses of other sectors that are useable,

causing the controller, in response to receipt from the processor of an address in a format designating at least one magnetic disk sector, to generate an address of a non-volatile memory sector that corresponds to said at least one magnetic disk sector,

accessing a usable sector of the memory system, if the sector with the generated address is unusable, by referring to the list to translate the unusable sector address into an address of another sector that is usable and then accessing that other sector,

either writing data to, or reading data from, the user data portion of the accessed usable sector, and

either writing to, or reading from, said overhead portion of the accessed usable sector, information related to either the accessed usable sector or data stored in the user data portion of

said accessed useful sector.--

--80. The method according to claim 79, wherein the detecting of the predefined condition includes detecting when individual sectors become defective.--

--81. The method according to claim 80, wherein the detecting of when individual sectors become defective includes determining when a number of individual defective memory cells within a sector exceed a given number.--

--82. The method according to claim 79, wherein the user data portion of the individual non-volatile memory sectors has a capacity of substantially 512 bytes.--

--83. The method according to claim 79, wherein the information stored in the overhead portion of the individual sectors includes an address of the respective ones of the individual sectors.--

--84. The method according to claim 79, wherein the information stored in the overhead portion of the individual sectors includes an error correction code for data stored in the user data portions of corresponding ones of the individual sectors.--

--85. A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the processor of an address in a format designating at least one

magnetic disk sector, to designate an address of at least one non-volatile memory sector that corresponds with said at least one magnetic disk sector,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory sector, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory sector.--

--~~86~~ 11. The method of claim ~~85~~ 10, wherein the user data portion of the individual sectors has a capacity of substantially 512 bytes.--

--~~87~~ 12. The method of claim ~~85~~ 10, wherein the overhead data stored in said overhead portion of the individual sectors includes addresses of the individual sectors.--

--88. The method of claim 85, ~~wherein~~ the partitioning step includes partitioning the memory cells within the individual sectors to include an additional portion of spare memory cells.--

--~~89~~ 14. The method of claim 88, wherein the overhead data stored in said overhead portion of the individual sectors includes an identification of any defective cells within the user data portion of corresponding ones of said sectors, said method additionally comprising causing the controller to read the identification of defective cells from the overhead portion of said addressed at least one non-volatile memory sector and then to substitute therefore other cells within the spare cell portion of the addressed at least one non-volatile memory sector.--

--90. The method of claim 85, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the array, and, wherein the sector addressing step includes, in response to designating an address of a defective sector, substituting an address of another sector instead.--

--16. The method of claim 12, wherein the individual sectors include only one user data portion and only one overhead data portion.--

--92. A memory system on a card that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and overhead data, and

means connectable to said computer system for controlling operation of the array, said controlling means including:

means responsive to receipt of a magnetic disk sector address from the host computer system for addressing a corresponding non-volatile memory sector,

means for reading the overhead data stored in the addressed sector, and

means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, writing user data to or erasing the addressed sector.--

--93. The memory system according to claim 92 wherein said controlling means additionally includes means listing any unusable ones of said plurality of non-volatile memory sectors for linking said unusable sectors with others of said sectors that are usable, and wherein said non-volatile memory sector addressing means includes means for accessing linked others of said sectors in place of said unusable sectors.--

--94. The memory system according to claim 92 wherein said given amount of user data is substantially 512 bytes.--

--95. The memory system according to claim 82 wherein said magnetic disk sector address includes a head, cylinder and sector.--

--96. The memory system according to claim 82 wherein the individual sectors of the memory array additionally have enough

cells for providing redundant cells in excess of that necessary to store said given amount of user data and said overhead data, said controlling means additionally including means for substituting redundant cells of a sector for any defective cells within the sector.--

--~~57~~ 72. The memory system according to claim ~~96~~ 21 wherein said substituting means including means referencing the overhead data of an addressed sector for substituting redundant cells within the addressed sector.--

REMARKS

This Second Preliminary Amendment is being filed prior to an Examiner's Action in the present continuation application. Claims 70-75, added by the first Preliminary Amendment filed on December 22, 1994, are being amended in order to keep them within the elected group of claims which parent application serial no. 07/963,838 (now patent no. 5,297,148) pursued. Other claims being added by this Amendment are also limited in the same manner. The parent application was in turn a division of earlier application serial no. 07/337,566, now abandoned. The parent pursued a Group IV of claims identified in a Requirement for Restriction dated July 15, 1991, in the earlier application. A related Group II of claims is being pursued in a copending application serial no. 08/249,049, also pending in Group Art Unit 2313.

A Supplemental Disclosure Statement, and copies of the references listed therein, were separately mailed to the Patent and Trademark Office, under a Certificate of Mailing, on January 5, 1995. A Second Supplemental Disclosure Statement, with copies of references cited, was similarly mailed on January 12, 1995.

An early examination and allowance of the present application, as twice preliminarily amended, is solicited.

Respectfully submitted,

Dated: February 10, 1995

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Atty. Docket: HARI-0606

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
ELIYAHOU HARARI, *et al.*	Group Art Unit: 2313
Serial No.: 08/174,768	
Filed: December 29, 1993	
For: FLASH EEPROM SYSTEM	San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING UNDER 37 CFR 1.10

I hereby certify that this patent application transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" Mailing Label Number TB614037633 addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on February 10, 1995.

Brenda J. Dolly
Signature — Date: 2/10/95

TRANSMITTAL OF SECOND PRELIMINARY AMENDMENT

Sir:

Transmitted herewith is an amendment in the captioned application. A check in the amount of $646.00 is enclosed to cover the fee for filing additional claims.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: February 10, 1995

Gerald P. Parsons, Reg. No. 24,486
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Atty. Docket: HARI-0606

08/174,768

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
	12/20/93	HARARI	

EXAMINER	
HUA, L	
ART UNIT	PAPER NUMBER
2413	8

2401/0518

PARSONS
PARSONS, HSUE & SIEBERT
[illegible] CENTER, SUITE 1450
[illegible] CA 94111-4121

DATE MAILED: 05/18/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on Feb. 10, 1995 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-62, and 63-94 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☑ Claims 1-62 have been cancelled.
3. ☑ Claims 79-94 and 95-97 are allowed.
4. ☑ Claims 63-67 and 70-78 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☑ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

SAN000792

EXAMINER'S ACTION

1. Claims 64-~~77~~ 69 are rejected under 35 U.S.C. § 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim.

As per claims 64-69:

These dependent claims refer to the memory system card which is not the invention set forth in parent claim 63. Notice that the parent claim claims a memory system, not the memory system card.

2. Claim 67 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 67:

A lines 1-2, the phrase "said memory card" lacks antecedent basis.

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claim 63-~~69~~ 78 are rejected under 35 U.S.C. § 103 as being unpatentable over Nozawa et al. (4,525,839, hereafter referred to as Nozawa).

As per claim 63:

Nozawa discloses the feature of defective sector substitution in a memory system substantially as claimed. Nozawa's memory system is connectable to a computer system and comprises:

an array (elements 11T and 13T and the sectors therein) of non-volatile memory cells partitioned into a plurality of sectors(n, n+1, n+2, n+3, ...; sectors N, N+1, N+2, N+3, ...) and that individually include a distinct group of the array of memory cells;

means (elements 60 and 70) for controlling operation of the array;

means (pointers 23a) for linking any defective ones of the plurality of sectors to others of the sectors; and

means (elements 50, 51, 61, 64, 63, 71, 76 and 77; see also step 130 shown in figure 6 or step 222 of figure 8; and

column 14, lines 24) for accessing linked others of the sectors in place of the defective sectors.

However, Nozawa does not teach that his memory system cells are of floating gate type. But Nozawa teaches that his system is of disk drive storage system type.

It would have been obvious to an artisan at the time the invention was made to apply Nozawa's feature of defective sector substitution into a memory system of floating gate type.

The artisan would have been motivated to apply Nozawa's feature into a floating gate memory system of because the group of floating gate memory cells in the floating gate memory system are prone to be defective and different features of defective memory area substitution have been used for replacing a defective memory cells in the floating gate memory with an alternate memory area.

As per claim 64:

Nozawa's linking means (23a) is stored in the array.

As per claim 65:

Nozawa's accessing means is within the controller (elements 60 and 70).

As per claim 66:

Nozawa teaches that his memory system is accessible by read and write commands issued by channel 51 which is understood to be

connected to the processor to which the memory system is connected.

As per claim 67:

Nozawa teaches that his feature can be applied to a recording system where the data is processed as a block and that the recording medium is of disk type. (Column 7, lines 55-59).

As per claim 68:

Nozawa's sector linking means is a list of defect pointers which map defective sectors into one of the others of the sectors. (See column 3, line 22, to column 4, line 34).

As per claim 69:

The means for adding a defect pointer to a list for mapping a particular sector into another sector is inherent in the system of Nozawa in order for the system of Nozawa to record (into pointer section 23a) the sector position of the sector which has been too many number of defective cells such that the read error cannot be corrected by the error correction code. (See column 3, lines 55-59).

As per claims 70 and 71:

Nozawa discloses the invention substantially as claimed. Nozawa's teaches a method of operating a computer system, more specifically a method of re-mapping defective memory sector. Nozawa's method comprises the step of:

providing an array (elements 11T and 13T and the sectors therein) of non-volatile memory cells partitioned into a plurality of sectors(n, n+1, .n+2, n+3, ...; sectors N, N+1, N+2, N+3, ...) and that individually include a distinct group of the array of memory cells;

providing means (elements 60 and 70) for controlling operation of the array;

identifying when a sector becomes defective (column 3, lines 55-59)

linking by the means (pointers 23a) for linking any defective ones of the plurality of sectors to others of the sectors; and

accessing by the means (elements 50, 51, 61, 64, 63, 71, 76 and 77; see also step 130 shown in figure 6 or step 222 of figure 8; and column 14, lines 24) for accessing linked others of the sectors in place of the defective sectors.

However, Nozawa does not teach that his memory system cells are of floating gate type. But Nozawa teaches that his system is of disk drive storage system type.

It would have been obvious to an artisan at the time the invention was made to apply Nozawa's feature of defective sector substitution into a memory system of floating gate type.

The artisan would have been motivated to apply Nozawa's feature into a floating gate memory system of because the group of floating gate memory cells in the floating gate memory system are prone to be defective and different features of defective memory area substitution have been used for replacing a defective memory cells in the floating gate memory with an alternate memory area.

As per claim 72:

Nozawa's linking means (23a) is stored in the array.

As per claim 73:

Nozawa's accessing means is within the controller (elements 60 and 70).

As per claim 74:

Nozawa teaches that his memory system is accessible by read and write commands issued by channel 51 which is understood to be connected to the processor to which the memory system is connected.

As per claim 75:

Identifying when a sector becomes detective by referencing to the number of defective cells such that the read error cannot be corrected by the error correction code is taught by Nozawa (see column 3, lines 55-59).

As per claim 76:

Nozawa teaches the storing of user data. The storing of overhead information would have been obvious to an artisan because Nozawa teaches storing information and overhead information is information which can be stored. The artisan would have been motivated to store the overhead information because the overhead information is informative.

As per claim 77:

Nozawa teaches the storing sector addresses in the individual sectors.

As per claim 78:

Nozawa teaches the storing of error correction codes.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly V. Hua whose telephone number is (703) 305-9684.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

L. Hua
April 14, 1998

ROBERT W. BEAUSOLIEL, JR.
SUPERVISORY PATENT EXAMINER
GROUP 2400

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 2-92) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED	08/174,768	2413	8
	APPLICANT(S) HAKARI ET AL.		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4380066	4/83	SPENCER ET AL	371	10.2	
	B	4525839	6/85	NOZAWA ET AL.	371	38.1	
	C	4463450	7/84	HAEUSELE	371	10.1	
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE	
Ly V Hua	4/15/95	SAN000800

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

PTO Draftpersons review all originally filed drawings regardless of whether they are designated as formal or informal. Additionally, patent Examiners will review the drawings for compliance with the regulations. Direct telephone inquiries concerning this review to the Drawing Review Branch, 703-305-8404.

The drawings filed (insert date) 12/29/93 are
A. ___ not objected to by the Draftsperson under 37 CFR 1.84 or 1.152.
B. ✓ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this Notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ___ Not black solid lines. Fig(s)_____
   - ___ Color drawings are not acceptable until petition is granted.

2. PHOTOGRAPHS. 37 CFR 1.84(b)
   - ___ Photographs are not acceptable until petition is granted.

3. GRAPHIC FORMS. 37 CFR 1.84 (d)
   - ___ Chemical or mathematical formula not labeled as separate figure. Fig(s)_____
   - ___ Group of waveforms not presented as a single figure, using common vertical axis with time extending along horizontal axis. Fig(s)_____
   - ___ Individuals waveform not identified with a separate letter designation adjacent to the vertical axis. Fig(s)_____

4. TYPE OF PAPER. 37 CFR 1.84(e)
   - ___ Paper not flexible, strong, white, smooth, nonshiny, and durable. Sheet(s)_____
   - ___ Erasures, alterations, overwritings, interlineations, cracks, creases, and folds not allowed. Sheet(s)_____

5. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable paper sizes:
   - 21.6 cm. by 35.6 cm. (8 1/2 by 14 inches)
   - 21.6 cm. by 33.1 cm. (8 1/2 by 13 inches)
   - 21.6 cm. by 27.9 cm. (8 1/2 by 11 inches)
   - 21.0 cm. by 29.7 cm. (DIN size A4)
   - ___ All drawing sheets not the same size. Sheet(s)_____
   - ___ Drawing sheet not an acceptable size. Sheet(s)_____

6. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Paper size

21.6 cm. X 35.6 cm (8 1/2 X 14 inches)	21.6 cm X 33.1 cm (8 1/2 X 13 inches)	21 cm X 27.9 cm. (8 1/2 X 11 inches)	21 cm. X 29.7 cm (DIN Size A4)
T .5.1 cm. (2")	2.5 cm. (1")	2.5 cm. (1")	2.5cm
L .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	2.5 cm
R .64 cm (1/4")	.64 cm (1/4")	.64 cm (1/4")	1.5 cm
B .64 cm (1/4")	.64 cm. (1/4")	64 cm (1/4")	1.0 cm.

Margins do not conform to chart above
Sheet(s)_____
___Top (T) ___ Left (L) ___Right (R) ___Bottom (B)

7. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes
   - ___ All views not grouped together. Fig(s)_____
   - ___ Views connected by projection lines. Fig(s)_____
   - ___ Views contain center lines. Fig(s)_____

Partial views. 37 CFR 1.84(h)(2)
   - ___ Separate sheets not linked edge to edge. Fig(s)_____
   - ___ View and enlarged view not labeled separately. Fig(s)_____
   - ___ Long view relationship between different parts not clear and unambiguous. 37 CFR 1.84(h)(2)(ii) Fig(s)_____

Sectional views. 37 CFR 1.84(h)(3)
   - ___ Hatching not indicated for sectional portions of an object. Fig(s)_____
   - ___ Hatching of regularly spaced oblique parallel lines not spaced sufficiently. Fig(s)_____
   - ___ Hatching not at substantial angle to surrounding axes or principal lines. Fig(s)_____
   - ___ Cross section not drawn same as view with parts in cross section with regularly spaced parallel oblique strokes. Fig(s)_____
   - Hatching of juxtaposed different elements not angled in a different way. Figs.____
   - Separate view. 37 CFR 1.84(h)(4)
   - ___ A separate view required for a [illegible]

Modified forms. 37 CFR 1.84(h)(5)
   - ___ Modified forms of construction must be shown in separate views. Fig(s)_____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ___ View placed upon another view or within outline of another. Fig(s)_____
   - ___ Words do not appear in a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s)_____

9. SCALE. 37 CFR 1.84(k)
   - ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s)_____
   - ___ Indication such as "actual size" or "scale 1/2" not permitted. Fig(s)_____
   - ___ Elements of same view not in proportion to each other. Fig(s)_____

10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
   - ___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (except for color drawings). Fig(s)_____

11. SHADING. 37 CFR 1.84(m)
   - ___ Shading used for other than shape of spherical, cylindrical, and conical elements of an object, or for flat parts. Fig(s)_____
   - ___ Solid black shading areas not permitted. Fig(s)_____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
   - ___ Numbers and reference characters not plain and legible. 37 CFR 1.84(p)(1) Fig(s)_____
   - ___ Numbers and reference characters used in conjuction with brackets, inverted commas, or enclosed within outlines. 37 CFR 1.84(p)(1) Fig(s)_____
   - ___ Numbers and reference characters not oriented in same direction as the view. 37 CFR 1.84(p)(1) Fig(s)_____
   - ___ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s)_____
   - ___ Numbers, letters, and reference characters do not measure at least .32 cm. (1/8 inch) in height. 37 CFR(p)(3) Fig(s)_____

13. LEAD LINES. 37 CFR 1.84(q)
   - ___ Lead lines cross each other. Fig(s)_____
   - ___ Lead lines missing. Fig(s)_____
   - ___ Lead lines not as short as possible. Fig(s)_____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
   - ✓ Number appears in top margin. Fig(s) 1A-7
   - ___ Number not larger than reference characters. Fig(s)_____
   - ___ Sheets not numbered consecutively, and in Arabic numerals, beginning with number 1. Sheet(s)_____

15. NUMBER OF VIEWS. 37 CFR 1.84(u)
   - ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s)_____
   - ___ View numbers not preceded by the abbreviation Fig. Fig(s)_____
   - ___ Single view contains a view number and the abbreviation Fig.
   - ___ Numbers not larger than reference characters. Fig(s)_____

16. CORRECTIONS. 37 CFR 1.84(w)
   - ___ Corrections not durable and permanent. Fig(s)_____

17. DESIGN DRAWING. 37 CFR 1.152
   - ___ Surface shading shown not appropriate. Fig(s)_____
   - ___ Solid black shading not used for color contrast. Fig(s)_____

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#9

JUL 1995

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Eliyahou Harari et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413

Examiner: L. Hua

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

1995 JUL 18 PM 4:00
GROUP 2400

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 25, 1995.

Brenda J. Dolly
Signature

7/25/95
Date

THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Third Supplemental Disclosure Statement to the Supplemental Disclosure Statements filed on or about January 5, 1995 and January 12, 1995, and the Disclosure Statement filed on or about December 22, 1994, submitted for the Examiner's consideration. Consideration of each of these documents and the making of each of them of record in the file are respectfully requested.

The required fee of $210.00 is being filed herewith. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

Dated: July 25, 1995

Respectfully submitted,

SAN000803

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Atty. Docket: HARI-0606

#9 Sheet 1 of 1

MAIL ROOM JUL 28 1995 PATENT TRADEMARK OFFICE

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI-0606	SERIAL NO. 08/174,768
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT ELIYAHOU HARARI et al.	
		FILED December 29, 1993	GROUP 2413

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
EWH	A5	4 3 5 4 2 5 3	10/1982	Naden	395	182.06	
EWH	A6	4 4 2 2 1 6 1	12/1983	Kressel et al.	365	185.09	
EWH	A7	4 4 5 0 5 5 9	5/1984	Bond et al.	395	182.04	
EWH	A8	4 6 5 4 8 4 7	3/1987	Dutton	395	182.04	
EWH	A9	4 7 3 3 3 9 4	3/1988	Burkhard	365	230.01	
EWH	A10	4 8 9 6 2 6 2	1/1990	Wayama et al.	395	185.00	
EWH	A11	4 9 4 5 5 3 5	7/1990	Hosotani et al.	395	185.00	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
EWH	B1	0 0 8 6 8 8 6	8/1983	European Patent Appln.	—	—	yes
EWH	B2	2 1 3 6 9 9 2	9/1984	UK Patent Appln.	—	—	yes
EWH	B3	0 2 2 0 7 1 8	5/1987	European Patent Appln.	—	—	yes
EWH	B4	0 2 4 3 5 0 3	11/1987	European Patent Appln.	—	—	yes
EWH	B5	0 3 0 0 2 6 4	1/1989	European Patent Appln.	—	—	yes
EWH	B6	A 5 5 7 7 2 3	1/1987	AU Patent Abridgement	—	—	yes
EWH	B7	WO 8 4 0 0 6 2 8	2/1984	PCT W.I.P.O.	—	—	yes
EWH	B8	A0 1 0 5 4 5 4 3	3/1989	Japanese Patent Abstrac	—	—	Yes
EWH	B9	A6 0 1 7 8 5 6 4	2/1986	Japanese Patent Abstrac	—	—	Yes

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

EWH	C1	Wilson, "1-Mbit flash memories seek their role in system design," Computer Design, Vol. 28, No. 5, pps. 30-32, (March 1989)

EXAMINER	DATE CONSIDERED
Ly V Huu	November 6, 1995

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

2400

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#10/D

In re Patent Application of)
ELIYAHOU HARARI et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413
Examiner: L. Hua

San Francisco, California 9/7/95

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 25, 1995.

Brenda J. Dolly
Signature

7/25/95
Date

P 30134 08/31/95 08174768 13-1030 030 103 246.00CH
P 30135 08/31/95 08174768 13-1030 030 104 240.00CH

AMENDMENT

Sir:

In response to the Examiner's Action dated May 18, 1995, please amend the above-identified patent application, as follows:

IN THE SPECIFICATION:

In the "Cross-Reference to Related Applications" section added to page one by the Continuation Application Transmittal herein, substitute --5,297,148,-- for "_,___,___," on line 3, and strike the entire second paragraph beginning with "The following related patents" at line 6 and ending with "Peripheral Card" on line 44.

IN THE CLAIMS:

Cancel claims 63-78, without prejudice.

~~79~~. (Amended) A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

detecting a predefined condition when individual sectors become unusable and [adding addresses of such unusable sectors to a list maintained within the card that links] linking the addresses of such unusable sectors [addresses] with addresses of other sectors that are useable,

causing the controller, in response to receipt from the processor of an address in a format designating at least one magnetic disk sector, to generate an address of a non-volatile memory sector that corresponds to said at least one magnetic disk sector,

accessing a usable sector of the memory system, if the sector with the generated address is unusable, by referring to the [list to translate the unusable sector address into an address of]

linked address of another sector that is usable and then accessing that other sector,

either writing data to, or reading data from, the user data portion of the accessed usable sector, and

either writing to, or reading from, said overhead portion of the accessed usable sector, information related to either the accessed usable sector or data stored in the user data portion of said accessed useful sector.

~~88~~ 13. (Amended) The method of claim ~~85~~ 10, wherein [the] partitioning [step] the memory cells includes partitioning [the] said memory cells within the individual sectors to include an additional portion of spare memory cells.

~~90~~ 15. (Amended) The method of claim ~~85~~ 10, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the array, and, wherein [the sector addressing step] designating an address of a sector includes, in response to designating an address of a defective sector, substituting an address of another sector instead.

~~92~~. (Amended) A memory system on a card that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and overhead data, and

means connectable to said computer system for controlling operation of the array, said controlling means including:

means responsive to receipt of a magnetic disk sector address from the host computer system for addressing a corresponding non-volatile memory sector,

means for reading the overhead data stored in the addressed sector, and

means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to, [or erasing] the addressed sector.

~~95~~ 20. (Amended) The memory system according to claim [82] ~~92~~ 17 wherein said magnetic disk sector address includes a head, cylinder and sector.

~~96~~ 21. (Amended) The memory system according to claim [82] ~~92~~ 17 wherein the individual sectors of the memory array additionally have enough cells for providing redundant cells in excess of that necessary to store said given amount of user data and said overhead data, said controlling means additionally including means for substituting redundant cells of a sector for any defective cells within the sector.

Add the following new claims:

--~~98~~ 7. The method according to claim ~~79~~ 1 wherein linking the address of unusable sectors with sectors that are useable includes maintaining a list within the card that links such unusable sectors with addresses of corresponding ones of the other sectors that are useable, and wherein accessing a usable sector

includes referring to the list to translate the address of the unusable sector into an address of a usable sector.--

--~~99~~ 98. The method according to claim ~~79~~ 1 wherein linking the address of such unusable sectors includes storing within individual ones of the defective sectors addresses of corresponding useable sectors, and wherein accessing a usable sector corresponding to an unusable sector includes referring to the useable sector address stored in the unusable sector.--

--100. The method of claim 85, additionally comprising causing the controller to identify any defective non-volatile memory sectors within the array and storing within any of said defective sectors addresses of corresponding ones of other sectors, and, wherein designating an address of a sector includes, in response to designating an address of a defective sector, reading the address in the defective sector of said corresponding other sector and then accessing data within such other sector instead of data within the defective sector.--

--101. A method of operating a computer system including a processor and a memory system, comprising:

providing said memory system as a module that that is connectable to the computer system and which includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors of cells that are individually erasable together as a unit,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead data portion,

in response to receipt from the processor of an address of at least one mass memory storage block, designating an address of at least one of said non-volatile memory sectors,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory sector,

either writing overhead data to, or reading overhead data from, said overhead portion of said at least one non-volatile memory sector, said overhead data being related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory sector, and

the memory cells of said at least one non-volatile memory sector having been erased together as a unit prior to writing user data or overhead data therein.--

--102. The method according to claim 101, wherein designating an address of at least one of said non-volatile memory sectors includes use of a controller that is provided as part of said module.--

--103. The method according to claim 101, wherein the overhead data written to the overhead data portion of the non-volatile memory sectors includes addresses of the individual sectors in which the addresses are stored.--

--104. The method according to claim 101, wherein the overhead data written to the overhead data portion of the non-volatile memory sectors includes error correction codes for data stored in corresponding user data portions of the individual sectors.--

--105. The method according to claim 101, wherein the overhead data written to the overhead data portion of individual ones of the non-volatile memory sectors includes, in a case where the a sector is unusable, an address of a usable sector as a substitute for the unusable sector.--

--106. The method according to claim 101, additionally comprising:

identifying when individual ones of the non-volatile memory sectors become unusable,

linking the addresses of the unusable sectors with addresses of sectors that are useable, and

accessing a non-volatile memory sector by, when the sector being accessed is unusable, referring to the linked address of a sector that is useable, thereby to remap the unusable sector into another sector that is useable.--

--107. The method according to claim 106, wherein linking the address of unusable sectors with sectors that are useable includes maintaining a list within the module that links such unusable sectors with addresses of corresponding ones of the other sectors that are useable, and wherein accessing a sector includes referring to the list to translate the address of the unusable sector into an address of a corresponding usable sector.--

--108. The method according to claim 106 wherein linking the address of such unusable sectors includes storing addresses of corresponding useable sectors within the overhead portion of individual ones of the unusable sectors, and wherein accessing a usable sector includes referring to the useable sector address stored in the unusable sector overhead portion.--

--109. The method according to any one of claims 106-108 wherein a non-volatile memory sector is identified to be unusable when it becomes defective.--

--110. The method according to any one of claims 101-108, wherein the user data portion of the individual sectors has a capacity of substantially 512 bytes.--

--111. The method according to any one of claims 101-108 wherein causing the controller to designate an address of at least one of said non-volatile memory sectors includes designating a unique sector address for individual ones of the mass memory storage block addresses received from the processor.--

--112. The method according to claim 101, wherein partitioning of the memory cells includes partitioning the memory cells within the individual sectors to include an additional portion of spare memory cells.--

--113. The method according to claim 101, wherein the overhead data stored in said overhead portion of the individual sectors includes an identification of any defective cells within the user data portion of corresponding ones of said sectors, said method additionally comprising causing the controller to read the identification of defective cells from the overhead portion of said addressed at least one non-volatile memory sector and then to substitute therefore other cells within the spare cell portion of said addressed at least one non-volatile memory sector.--

--114. The method according to claim 101, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the module, and wherein designating an address of at least one of said non-volatile

memory sectors includes, in response to designating an address of a defective sector, substituting an address of another sector instead.--

--115. The method according to claim 114 wherein identifying when a sector becomes defective includes identifying when a sector has a number of defective memory cells therein which exceeds a given number.--

--116. A memory system unit having electrical terminations for establishing a connection with a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and some overhead data, and

a memory controller connected between said electrical terminations and said memory cell array for controlling operation of the array, said controller including:

means responsive to receipt of one or more mass memory storage block addresses through said terminations for addressing one or more of the non-volatile memory sectors, said addressing means including means responsive to an identification of any of the non-volatile memory sectors that are unusable for substituting another usable sector therefor,

means for reading overhead data stored in the addressed sector, and

means responsive to the read overhead data for either reading user data from, or writing user data to, ~~the addressed sector~~.--

--~~117~~ 24. The memory system according to claim ~~116~~ 23 wherein the identification of any unusable sectors includes a list maintained within the memory system unit that links addresses of unusable sectors with corresponding usable sectors.--

--~~118~~ 25. The memory system according to claim ~~116~~ 23 wherein the identification of any unusable sectors includes a record of individual addresses of substitute usable sectors stored as part of the overhead data in respective ones of the unusable sectors.--

--~~119~~ 26. The memory system according to any one of claims ~~116-118~~ 23-25 wherein the identification of any unusable sectors includes inoperable or defective sectors.--

--~~120~~ 27. The memory system according to any one of claims ~~116-118~~ 23-25 wherein the identification of any unusable sectors includes ~~sectors~~ that contain a number of defective cells in excess of a preset number.--

--~~121~~ 30. The memory system according to claim ~~116~~ 23 wherein said individual non-volatile memory sectors additionally have redundant memory cells in excess of that necessary to store said given amount of user data and said overhead data, said controller additionally including means for substituting redundant memory cells of an individual sector for defective memory cells within the individual sector.--

--~~122~~ 31. The memory system according to claim ~~116~~ 23 wherein the overhead data reading means includes means for reading from the overhead data of an addressed sector an address of that sector, and

wherein the controller additionally includes means for comparing the read overhead data address with the address of the sector, thereby to confirm that the desired sector has been addressed.--

--~~123~~ 32. The memory system according to any one of claims 23-25 ~~116-118~~, ~~121~~ 30 and ~~122~~ 31 wherein the given amount of user data that is storable in individual sectors is substantially equal to a size of individual mass memory storage blocks of the host computer system, and wherein the addressing means maps addresses of individual ones of the mass memory storage blocks into unique individual ones of the non-volatile memory sectors.--

--~~124~~ 28. The memory system according to any one of claims ~~103-124~~ 23-25 ~~116-118~~ wherein said given amount of user data is substantially equal to 512 bytes.--

--~~125~~ 29. The memory system according to any one of claims ~~116-118~~ 23-25 wherein said controller additionally includes means for selecting a plurality of sectors for an erase operation, and means for simultaneously performing an erase operation on only the selected plurality of sectors.--

--~~126~~ 33. The memory system according to any one of claims ~~116-118~~ 23-25, ~~121~~ 30 and ~~122~~ 31 wherein said memory system unit is implemented on a single printed circuit card.--

--~~127~~ 34. The memory system according to any one of claims ~~116-118~~ 23-25, ~~121~~ 30 and ~~122~~ 31 wherein the one or more mass memory storage block addresses to which the controller addressing means is responsive consists of one or more magnetic disk sector addresses.

REMARKS

The undersigned attorney appreciates the telephone interview granted by Examiner Hua on May 25, 1995, in order to clear up some inconsistencies in the outstanding Examiner's Action dated May 18, 1995. It was concluded that the summary designations of allowed and rejected claims in the cover sheet (line 3), page 2 (line 1) and page 3 (first line of para. 4) are in error. The correct status is as follows: Claims 79-97 stand allowed, claims 64-69 were rejected under 35 U.S.C. 112, and claims 63-78 were rejected under 35 U.S.C. 103 over the Nozawa *et al.* patent no. 4,525,839. It is with this understanding of the Examiner's Action that this responsive Amendment has been prepared and is being filed.

All of the rejected claims 63-78 are being cancelled without prejudice. The allowance of claims 79-97 is appreciated. Upon further review of the allowed claims, certain amendments to them have appeared to be desirable. Independent claim 79 is being amended to more generically describe the techniques disclosed in the present application for linking addresses of usable and unusable sectors, and then dependent claims 98 and 99 are being added to define two of those techniques. Editorial changes are being made to dependent claims 88 and 90. The amendment to allowed independent claim 92 eliminates reference to an erasing operation. It is expected that these few minor changes will not require reconsideration of the allowed claims.

In addition to new dependent claims 98 and 99, mentioned above, claims 100-127 are being added by this amendment. Claim 100 is dependent upon allowed independent claim 85, which is not being

amended in any way. Method claim 101 is one of only two independent claims being added, system claim 116 being the other. Claim 101 is similar to allowed claim 85 but is has a somewhat different scope. In a similar way, new independent system claim 116 corresponds to allowed claim 92. Since the essential novel features of the allowed claims are retained in new claims 101 and 116, they, and their dependent claims 102-115 and 117-127, are submitted to be allowable.

A Third Supplemental Disclosure Statement is being filed with this Amendment.

An early formal allowance of this application is solicited. However, if the Examiner has any further matters which require resolution, he is invited to telephone the undersigned attorney in order that they may be resolved as expeditiously as possible.

Respectfully submitted,

Dated: July 25, 1995

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Attorney for Applicant

Atty. Docket: HARI-0606

H66-113 2413

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
ELIYAHOU HARARI et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413
Examiner: L. Hua

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 25, 1995.

Brenda J. Dolly

Brenda J. Dolly 7/25/95
Signature Date

AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is an amendment in the captioned application.

A check in the amount of $766.00 is enclosed to cover the fee for filing additional claims.

Enclosed is a Third Supplemental Information Disclosure Statement, PTO 1449 with references, to be made of record in the above-referenced file. Also enclosed is a check in the amount of $210 to cover the filing fee.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment,

to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: July 25, 1995

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Atty. Docket: HARI-0606

Lee 24P1 2401 9/7/95 2413

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#11

In the Patent Application of	Group Art Unit:
ELIYAHOU HARARI et al.	Examiner: L. Hoa
Serial No.: 08/174,768	
Filed: December 29, 1993	
For: FLASH EEPROM SYSTEM	San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Supplemental Information Disclosure Statement submitted for the Examiner's consideration. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, are respectfully requested.

I hereby certify that no item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in §1.56(c) more than three months prior to the filing of this statement.

Respectfully submitted,

Dated: September 14, 1995

Gerald P. Parsons, Reg. No. 24,486
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Atty. Docket: HARI-0606

#11 Sheet 1 of 1

FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI-0606	08/174,768
	INFORMATION DISCLOSURE STATEMENT	APPLICANT	
		Eliyahou Harari et al.	
	(Use several sheets if necessary)	FILED	GROUP
		December 29, 1993	

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LdL	A12	4 2 9 5 2 0 5	10/1981	Kunstadt	395	410	
LdL	A13	4 6 1 7 6 2 4	10/1986	Goodman	395	402	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

EXAMINER	DATE CONSIDERED
L. V. Ilua	November 6, 1995

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.


12

#12

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
ELIYAHOU HARARI et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413
Examiner: L. Hua
San Francisco, California

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Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Supplemental Information Disclosure Statement submitted for the Examiner's consideration. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, are respectfully requested.

In a Third Supplemental Disclosure Statement, filed July 28, 1995, a complete (35 pages of text and Figures 1-8) copy of Australian patent application no. 22536/83 of Kevin John Burke, published under no. A557,723, was filed. However, it was referenced on the form PTO 1449 only as an "AU Patent Abridgement," the caption of a one-page abstract that was also filed with the complete patent application. Consideration of the full patent application, and the making it of record, are respectfully requested.

I hereby certify that no item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in §1.56(c) more than three months prior to the filing of this statement.

Respectfully submitted,

Dated: October 6, 1995

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Atty. Docket: HARI-0606

#12

FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI-0606	08/174,768
INFORMATION DISCLOSURE STATEMENT		APPLICANT	
		Eliyahou Harari	
(Use several sheets if necessary)		FILED	GROUP
		December 29, 1993	2413

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LW	A14	4 2 1 0 9 5 9	7/1980	Wozniak	395	894	
LW	A15	4 6 4 2 7 5 9	2/1987	Foster	395	500	
LW	A16	4 4 5 6 9 7 1	6/1984	Fukuda et al.	395	502	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

LW	C2	Miller, "Semidisk Disk Emulator," INTERFACE AGE, p. 102, November, 1982
LW	C3	Clewitt, "Bubble Memories as a Floppy Disk Replacement," 1978 MIDCON Technical Papers, Vol. 2, pp. 1-7, Dec. 1978
LW	C4	Hancock, "Architecting a CCD Replacement for the IBM 2305 Fixed Head Disk Drive," Digest of Papers, Eighteenth IEEE Computer Society International Conference, pp. 182-184, 1979

EXAMINER	DATE CONSIDERED
Ly V. Hua	November 6, 1995

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

08/174,768

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/174,768	12/29/93	HARARI	E HARI0606

EXAMINER	
HUA, L	
ART UNIT	**PAPER NUMBER**
2413	13

24M1/1207

GERALD P. PARSONS
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SAN FRANCISCO, CA 94111-4121

DATE MAILED: 12/07/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on July 28, 1995 Sept. 15, 1995 and Oct. 10, 1995 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1 - 127 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☑ Claims 1 - 78 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 79 - 127 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☑ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

1. Claims 101-115 and 116-127 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 101-115:

At line 3, claim 101, the word "that" is repeated.

At line 13, claim 101, the phrase "said non-volatile memory sectors" lacks antecedent basis.

As per claim 105:

The phrase "the a" is not idiomatic.

As per claim 113:

The phrase "the spare cells portion" lacks antecedent basis.

As per claim 116-127:

At line 3, claim 116, the phrase "said memory system" lacks antecedent basis.

2. The above rationales for the rejection under 35 U.S.C. 112, second paragraph, are only exemplary examples indicating that the claims contain problems of indefiniteness. The Applicant is, hereby, requested to review each of the pending claims and correct all indefinite problems if found.

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having

ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 85, 91, 101, 102 and 111 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) in view of Yorimoto et al (0-220-718 hereinafter referred to as Yorimoto).

As per claims 85, 91, 101, 102 and 111:

Burke teaches a computer system including (1) a processor and (2) a memory system. Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to "emulate" a magnetic disk which has sectors. To operate his computer system, Burke provides the array, and a controller. Burke's controller is within a board and is for controlling the operation of the array. Burke's controller is caused, when it receives from the processor an address designating a sector of the magnetic disk. Burke's cells are written with information.

Yorimoto teaches partitioning the cells with a sector into portions, each portion is for storing a specific type of information.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Yorimoto's memory (of EEPROM type) and Yorimoto's memory cells partitioning in place of Burke's memory.

The artisan would have been motivated to use Yorimoto's EEPROM in the place of Burke's memory because Yorimoto's EEPROM can be partitioned into sectors and Burke's

emulation inherently suggests that the emulating memory should be able to emulate the sectors of Burke's magnetic disk.

5. Claims 79-84, 86-90, 98-100, 103-105, 107-110, 112-115 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) in view of Yorimoto et al (0-220-718 hereinafter referred to as Yorimoto) and Satoh et al (4,774,700 hereinafter referred to as Satoh).

As per claim 79:

Burke teaches a computer system including (1) a processor and (2) a memory system. Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to "emulate" a magnetic disk which has sectors. To operate his computer system, Burke provides the array, and a controller. Burke's controller is within a board and is for controlling the operation of the array. Burke's controller is caused, when it receives from the processor an address designating a sector of the magnetic disk. Burke's cells are written with information.

Yorimoto teaches partitioning the cells with a sector into portions, each portion is for storing a specific type of information.

Satoh teaches replacing of defective sector with usable sector. Satoh's sector replacing operation includes detecting of an unusable sector, linking the address of the unusable sector with the address of the usable sector, and accessing the usable sector.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Yorimoto's memory (of EEPROM type) and Yorimoto's memory cells partitioning in place of Burke's memory and to apply Satoh's operation of sector replacing

to replace defective sector in Yorimoto's memory which has been used in the replace Burke's memory.

The artisan would have been motivated to use Yorimoto's EEPROM in the place of Burke's memory because Yorimoto's EEPROM can be partitioned into sectors and Burke's emulation inherently suggests that the emulating memory should be able to emulate the sectors of Burke's magnetic disk. The artisan would have also been motivated to use Satoh's operation of replacing defective sector in the modified memory system of Burke because the EEPROM replacing Burke's memory is prone to be defective and because Satoh's operation enhances fault tolerance.

As per claims 80 and 109:

Satoh teaches detecting a condition when a sector become defective.

As per claims 83, 87, 84, 103, 104 and 105:

It would have been obvious to one having ordinary skill in the art at the time the invention was made realize that addresses of defective sectors, error correction code and addresses of substitute sectors are information which can be written into (or read from) the overhead portions of a memory device.

As per claims 88 and 112:

Satoh's cells which are used for replacing his defective sectors are spare cells.

As per claims 82, 86 and 110:

The size of 512-bytes, which is took as a given amount of user data, is of obvious design choice.

As per claim 81 and 115:

Official notice is, hereby, taken that it is notoriously old and well known in the art to identify a bad group of cells, when the number of defective memory cells within the group of cells is greater than a preset number and the number of bit errors in the group of cells is beyond the capability of correcting by using error correction code, so that this group of cells can be replaced with an alternative group of cells.

As per claims 89, 98, 99, 90, 100, 106, 107, 108, 113 and 114:

Official notice is, hereby taken that:

a. linking the address of unusable sector with address of useable sector by storing address of corresponding useable sector,

b. identifying defective sector and storing addresses of defective sector, and

c. including, as overhead data, an identification of defective cells within the user data portion; and

d. accessing a usable sector by (1) referring to the useable sector address stored in the unusable sector and (2) referring to the list to translate the address of the unusable sector into an address of a usable sector,

e. causing the controller (1) to read the identification of defective cells and then (2) to substitute therefore other cells within the spare cell portion, and

f. designating an address of a sector by (1) substituting an address of another sector and (2) reading the address of a corresponding sector and then accessing data within such other sector

are notoriously old and well known in the art of memory patching.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate (1) those conventional features of address translation for

referring to useable sector (or cells) instead of defective sector (or cells) and (2) those conventional features of mapping unusable sector (or cells) into useable sector (or cells) into the modified system of Burke. The artisan would have been motivated to incorporate these memory patching features into the modified system of Burke because:

a Burke teaches (1) translating of address signals so as to access an alternative memory location instead of memory location which is to be avoided and (2) emulating a magnetic memory by using a semiconductor memory;

b semiconductor memories (e.g. Yorimoto's EEPROM) are prone to be defective,

c memory patching allows fault tolerance for defect in memory locations, and

d Yorimoto teaches usage of good memory location instead of defective memory location.

6. Claims 92, 116, 118-120, 122, 123, 125-127 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) in view of Yorimoto et al. (0-220-718 hereinafter referred to as Yorimoto).

As per claim 92:

Burke teaches a memory system that is connected to a host computer and is comprising: (a) a semiconductor memory; and (b) electronic control means, which is connectable to said computer, for controlling operation of the semiconductor memory. Burke 's semiconductor memory reads on Applicant's array of memory cells. Burke 's electronic control means reads on Applicant's means for controlling the operation the array. Burke 's electronic control means includes circuit means, which reads on Applicant's means for

addressing, for translating address signals, which are from the host computer for the magnetic memory device, to corresponding address signals for the semiconductor memory.

Burke, however does not explicitly teach that his semiconductor memory is of "non-volatile floating-gate" type. Burke also does not explicitly cite that his memory cells are partitioned into a plurality of sectors that individually include a distinct group of memory cells that are erasable together as a unit. Furthermore Burke does not explicitly cite that his memory cells are for storing a given amount of user data and overhead data. Burke does not explicitly cite that his address signals, which are from the host computer for the magnetic memory device, are sector address signals. Burke also does not explicitly recite that his corresponding address signals are addressing a corresponding nonvolatile memory sector. Burke also does not explicitly teach means for reading the overhead data stored in the addressed sector, and means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to the addressed sector. But Burke does teaches that his memory system has reading/writing means.

It is understood that (a) Burke's address signals, which are from the host computer for the magnetic memory device, are sector address signals, and (b) Burke's corresponding address signals, which have been derived from translating the sector address signals, are equivalent to that of sector address signals because Burke's semiconductor memory is emulating his magnetic memory device. It is also understood that Burke's memory cells are being partitioned into a plurality of sectors, each of which includes a distinct group of memory cells that are erasable together as a unit, because Burke's semiconductor memory is emulating his magnetic memory device. Besides this understanding, partitioning of nonvolatile

memory cells into a plurality of nonvolatile memory sectors that individually include a distinct group of memory cells that are erasable together as a unit is known in the art (see Yorimoto example),

Official notice is, hereby, taken that: (1) providing, in a sector, enough memory cells for storing a given amount of user data and overhead data; (2) means for reading the overhead data stored in the addressed sector; and (3) means responsive to the read overhead data, (such as validity check bit information, or remapping information), for reading user data from or writing user data to the user data field of the sector, which has the overhead data field in which the overhead data is stored, are notoriously old and well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to:

a. realize that Burke's address signals, which are from his host computer for addressing his magnetic memory device, are sector address signals **because** magnetic memory devices are addressed according to sectors;

b. realize that Burke's corresponding address signals, which have been derived from translating the sector address signals, are equivalent to that of sector address signals **because** a translating of one identify must be equivalent to that identify and because Burke's semiconductor memory is emulating his magnetic memory device and those signals which are applied to the emulating device are equivalent to those signals which are applied to the emulated device;

c. realize that Burke's memory cells are being partitioned into a plurality of sectors **because** his memory cells are emulating his magnetic memory device's bit-storing units;

d. realize that each of Burke's information bits in a group of his memory cells are erasable together as a unit **because** Burke's semiconductor memory is emulating his magnetic memory device and it is known in the art that the information bits in a group of bit-storing units (called sector) in a magnetic memory device are erasable together as a unit;

e. replace Burke's semiconductor memory device with nonvolatile memory device, such as that of Yorimoto, **because** nonvolatile memory device would emulate magnetic memory device better since magnetic memory device is nonvolatile;

f. provide, in a sector, enough memory cells for storing a given amount of user data and overhead data **because** otherwise the sector would not able to store all of the necessary amount of information which is to be stored in that sector;

g. provide means for reading the overhead data stored in the addressed sector **because** this overhead data is needed first in order to determine whether the user data in the user data fields are valid or not and whether any field has been remapped; and

h. provide means, responsive to the read overhead data (such as validity check bit information, or remapping information), for reading user data from (or writing user data to) the user data fields of the sector, which has the overhead data field in which the overhead data is stored **because** the objective of accessing

the emulating semiconductor memory device is to read data from or to write data to it.

The artisan would have been motivated to realize the points indicated above because Burke the usage of semiconductor memory device for emulating a magnetic memory device. The artisan would have also been motivated to replace Burke's semiconductor memory device with Yorimoto's nonvolatile memory device because Yorimoto's nonvolatile memory device is capable of being partitioned into sectors which would be suitable for simulating the sectors of a magnetic memory device and suitable for simulating the nonvolatile characteristic of the magnetic memory device. The artisan would also have been motivated to provide the appropriate means in order to properly read information from or write information to the appropriate sector field in the addressed sector because properly read information from and write information to memory device by using overhead information such as error/validity bit information and/or remap information are known in the art of memory fault detection and correction.

As per claims 116 and 123:

Burke's memory system, being connected to his host computer, has electrical terminations for establishing a connection with the host computer. Burke's controller, which is in his memory system, is connected to his host computer. From this connection, it is readily understood that Burke's controller is connected between his electrical terminations and his memory cell array.

As per claim 118:

Official notice is, hereby, taken that storing addresses, which indicate substitute usable memory location, together with other header information such as defect indicating flag is

notoriously old and well known in the art of address translation for the purpose of substituting alternative memory location for defective main memory location.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to the identify unusable sectors and identify, by using address information, the substitute usable sectors so that when an unusable sector is accessed it can be substituted with a usable sector.

One having ordinary skill in the art would be motivated to store the addresses of alternative sector in the header information field because these addresses would refer an access to a substitute memory location and because Yorimoto teaching does relate to substitution of defective memory sector.

As per claim 119:

Yorimoto teaches that unusable memory sectors are those sectors which are defective.

As per claim 120:

Official notice is, hereby, taken that it is notoriously old and well known in the art to identify a bad group of cells, when the number of defective memory cells within the group of cells is greater than a preset number and the number of bit errors in the group of cells is beyond the capability of correcting by using error correction code, so that this group of cells can be replaced with an alternative group of cells.

As per claim 122:

The technique of verifying the validity of addressing a memory location as claimed in this claim is notoriously old and well known in the art of memory accessing checking.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to check whether addressing is valid or not because getting incorrect data

from a memory could be caused by accessing a wrong location due to the error in the address information.

As per claim 125:

Official notice is, hereby, taken that distribution of the segments of a large file among a plurality of memory sectors is notoriously old and well known in the art of storing information. Official notice is also, hereby, taken that it is notoriously old and well known that upon erasing the large file, which has been distributed among a plurality of memory sectors, the plurality of memory sectors must be selected and erased in order for the large file to be completely erased.

As per claim 126:

It would have been obvious to an artisan in the art at the time the invention was made to implement Burke's memory system in a single printed circuit card because the advancement in the technology of semiconductor has encouraged artisans to implement many components of a system into a single printed circuit card so as to modularize the system and to have a more compact unit of the system.

As per claim 127:

Burke's memory system emulates a magnetic memory and translates the address addressing the magnetic memory in order to address the emulating semiconductor memory.

7. Claims 93-97, 117, 121, 124 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) and Yorimoto (JP0-220-718) as applied to claims 92 and 116 above, and further in view of Nozawa et al (4,525,839 hereinafter referred to as Nozawa).

As per claims 93 and 117:

In a memory system, Nozawa teaches means (i.e. pointers 23a) listing any unusable ones of a plurality of non-volatile memory sectors for linking the unusable sectors with others of sectors that are usable. Nozawa also teaches, in non-volatile memory-sector addressing means, means (elements 50, 51, 61, 64, 63, 71, 76, and 77) for accessing linked others of said sectors in place of said unusable sectors.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to: (1) use, in Burke's memory system, Nozawa's pointer linking least means for listing memory sector, which cannot be used due to defect, so that the pointers in this pointer linking least means can refer the accessing to an alternate sector which can be used; and (2) provide, in Burke's memory system, Nozawa's means for accessing the alternate sector in place of the defective sector.

The artisan would have been motivated to utilize Burke's pointer linking list means and provide the means for accessing the alternate sector in Burke's memory system because memory patching by method of remapping is notoriously old and well known in the art and because Yorimoto's memory in Burke's modified memory system is prone to be defective and utilization and the provision would provide tolerance to that defect.

As per claims 94 and 124:

The size of 512-bytes, which is took as a given amount of user data, is of obvious design choice.

As per claim 95:

Head, cylinder and sector are well known information fields which are associated with addresses for addressing magnetic disk sector.

As per claims 96 and 121:

Nozawa teaches accessing alternative blocks for defective blocks upon detection of defect in the defective block, thus suggests a controlling means for controlling a substitution.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide, for the purpose of sufficiency, enough redundant memory cells in order to adequately store those information which cannot be stored in the main cells in case the main cells become defective.

As per claim 97:

Official notice is, hereby, taken that header information including defect descriptor comprising defect pointer, which is referred to in order to skip bad memory location and jump to an alternative location for the purpose of replacing the bad memory location is notoriously old and well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that it is necessary to provide a referencing means in order to refer to the overhead data (i.e. the defect pointer) in order to determine whether or not the main memory cells need substitution.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr., can be reached on (703) 305-9713. The fax phone number for this Group is (703) 305-9600.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9724.

L. Hua
November 9, 1995

ROBERT W. BEAUSOLIEL, JR.
SUPERVISORY PATENT EXAMINER
GROUP 2400

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 2-92)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER	
NOTICE OF REFERENCES CITED		08/174,768	2413		13
		APPLICANT(S) HARARI ET AL.			

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	5226168	7/93	KOBAYASHI ET AL	395	800	
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

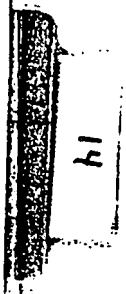
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE	
Ly Hua	11/8/95	SAN000845

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)



#900-117 GR5413

#14

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
ELI HARARI et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413

Examiner: L. Hua

San Francisco, California

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Amendments Commissioner of Patents and Trademarks, Washington, D.C. 20231 on June 7, 1996.

Brenda J. Dolly

Brenda J. Dolly 6/07/96

Signature Date

PETITION FOR EXTENSION OF TIME

Sir:

It is hereby petitioned that a three-month extension of time be granted in order to respond to the Office Action dated December 7, 1995. This response extends the deadline for response until June 7, 1996.

A check in the amount of $900.00 is attached to cover the extension fee.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 13-1030.

Respectfully submitted,

Dated: June 7, 1996

Gerald P. Parsons

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Atty. Docket: HARI-0606

#78-102 GR 2413

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#15/E

In the Patent Application of)
ELIYAHOU HARARI et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413
Examiner: L. Hua

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Amendments Commissioner of Patents and Trademarks, Washington, D.C. 20231 on June 7, 1996.

Brenda J. Dolly
Brenda J. Dolly 6/07/96
Signature Date

AMENDMENT

Sir:

In response to the Examiner's Action dated December 7, 1995, please amend the above-identified patent application as follows:

IN THE CLAIMS:

Cancel claims 100-115 without prejudice.

Amend claims 84, 92 and 116, as follows:

~~84~~ 68. (Amended) The method according to claim ~~79~~ 1, wherein the information stored in the overhead portion of the individual sectors includes an error correction code [for] calculated from data stored in the user data portions of corresponding ones of the individual sectors.

OK refund 6/10/96

17~~92~~. (Twice Amended) A memory system on a card that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and overhead data, and

means connectable to said computer system for controlling operation of the array, said controlling means including:

means responsive to receipt of a magnetic disk sector address from the host computer system for addressing a corresponding non-volatile memory sector,

means for reading the overhead data stored in the addressed sector prior to either reading the user data from, or writing user data to, the addressed sector, and

means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to, the addressed sector.

23~~16~~. (Amended) A memory system [unit] having electrical terminations for establishing a connection with a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and some overhead data, and

a memory controller connected between said electrical terminations and said memory cell array for controlling operation of the array, said controller including:

means responsive to receipt of one or more mass memory storage block addresses through said terminations for addressing one or more of the non-volatile memory sectors, said addressing means including means responsive to an identification of any of the non-volatile memory

sectors that are unusable for substituting another usable sector therefor,

means for reading overhead data stored in the addressed sector prior to either reading the user data from, or writing user data to, the addressed sector, and

means responsive to the read overhead data for either reading user data from, or writing user data to, the addressed sector.

Add the following new claims:

35. In a computer system including a processor and a memory system, wherein the memory system includes an array of integrated electronic circuit non-volatile floating gate memory cells partitioned into a plurality of distinct sectors of said memory cells that are individually erasable together as a unit separately from other sectors, a method of operating the memory system, comprising:

removably connecting said memory system including a controller to the computer system in a manner that said controller communicates with said processor for controlling operation of the array,

in response to receipt from the processor of an address in a format designating at least one mass memory storage block, generating through the controller (1) an address of at least one of said plurality of sectors of non-volatile memory corresponding to said at least one mass memory storage block and (2) an erase, write or read command,

in response to an erase command, erasing said at least one sector,

in response to a write command, reading, from an overhead portion of said at least one sector, overhead data of a characteristic of said at least one sector, and thereafter writing user data in the user data portion of said at least one sector and writing a characteristic of the written user data in the overhead portion of said at least one sector, and

in response to a read command, reading, from an overhead portion of said at least one sector, overhead data of a

characteristic of said at least one sector or of data stored in the user data portion of said at least one sector, and thereafter reading data from the user data portion of said at least one sector.

36
~~129~~. The method of claim 35 ~~128~~, which additionally comprises storing within the memory system links from addresses of any unusable sectors to addresses of others of said plurality of sectors, and wherein generating an address of said at least one of said plurality of sectors includes referring to said address links to substitute an address of a useable sector for an address of an unusable sector.

37 ~~130~~. The method of claim 36 ~~129~~ the address links are stored for sectors that are unusable by reason of more that a predetermined number of memory cells therein being defective.

38 ~~131~~. The method of claim 36 ~~129~~ wherein any links to addresses of useable ones of said plurality of sectors are stored in the overhead portion of unusable ones of said plurality of sectors.

39 ~~132~~. The method of claim 35 ~~128~~ wherein erasing said at least one sector includes simultaneously erasing two or more but less than all of said plurality of sectors.

40 ~~133~~. The method of claim 35 ~~128~~ wherein generating an address of said at least one sector includes generating addresses of a number of said plurality of sectors that is equal to a number of mass memory storage block addresses received from the processor.

41 ~~134~~. The method of claim 40 ~~133~~, wherein the user data portion of the individual sectors has a capacity of substantially 512 bytes.

42 ~~135~~. The method of claim 35 ~~128~~, wherein the overhead data stored in said overhead data portion of said at least one sector includes the address of said at least one sector.

43 ~~136~~. The method of claim 42 ~~135~~, wherein, in response to either the write command or the read command, overhead data that is read includes the address of said at least one sector.

44 ~~137~~. The method of claim 43 ~~136~~, wherein the address read from the overhead portion of said at least one sector is compared with the address that was generated through the controller.

45 ~~138~~. The method of claim 35 ~~128~~, wherein the overhead data stored in said overhead data portion of said at least one sector includes, if said at least one sector is defective, an address linking said at least one sector to another of said plurality of sectors.

46 ~~139~~. The method of claim 45 ~~138~~, wherein generating an address of said at least one of said plurality of sectors includes referring to said address linking to substitute an address of a useable sector for an address of an unusable sector.

47 ~~140~~. The method of claim 35 ~~128~~, wherein the overhead data stored in said overhead portion of said at least one sector includes an identification of any defective cells within the user data portion of said at least one sector.

48 ~~141~~. The method of claim 47 ~~140~~, additionally comprising, in response to either the write command or the read command, reading through the controller the identification of defective cells from the overhead portion of said at least one sector and then substituting therefore other cells within the said at least one sector.

49 ~~142~~. The method of claim 35 ~~128~~, wherein the writing of a characteristic of the user data includes calculating an error correction code from the written user data and writing said error correction code into the overhead portion of said at least one sector.

50 ~~143~~. The method of claim 35 ~~128~~, wherein said at least one mass memory storage block sector address received from the processor includes a head, cylinder and sector.

9 ~~144~~. The method according to claim 1 ~~29~~, wherein causing the controller to generate an address of a non-volatile memory sector includes doing so for a non-volatile memory sector that corresponds to only one magnetic disk sector, wherein the user data portion of the individual non-volatile memory sectors has a capacity that is substantially the same as a user data portion of said one magnetic disk sector.--

REMARKS

The preamble of claim 116 has been amended in response to the rejection of claims 116-127 under 35 U.S.C. 112, second paragraph. Since claims 101-115 are being cancelled, this is the only section 112 rejection to which a response is necessary.

The rejections of the remaining claims in this application over various combinations of prior art under 35 U.S.C. 103 are discussed below. The following cited prior art is discussed below: Australian patent no. 22536/83 ("Burke"), European patent application publication no. 0 220 718 ("Yorimoto *et al.*"), and U.S. patents nos. 4,774,700 ("Satoh *et al.*") and 4,525,839 ("Nozawa *et al.*"). For the reasons stated below, it is respectfully submitted that the cited references would not have rendered the claims of the present application obvious to one ordinarily skilled in the art before April 13, 1989, the effective filing date of the present application.

Summary of Argument

The claims are directed to a flash EEPROM system, or to the use and operation of such a memory system, that includes its own controller. The memory controller both makes it possible for the host system to communicate with the memory system and controls operation of the flash EEPROM cell array. The memory cell array is divided into sectors, with the cells within each sector being erasable together as a unit. Stored in each sector is a sectors worth of user data and some overhead information (a header) about the sector and/or about the user data stored in the sector.

The claimed memory system looks to the host computer as if it was a disk drive system, similar to the goal stated in the cited Burke patent. But a significant difference is the claimed operation of the flash EEPROM array with many incidents of a disk system. It is divided into sectors that are operated as a unit, including overhead data (a header) as well as user data, and, in some of the claims, the overhead data is read from an addressed sector before user data is written into that sector.

This is quite different from the way that semiconductor memory arrays are usually operated. Data is usually written to or

read from a RAM by first addressing one storage location, holding one or a few bytes of data, and then incrementing through adjacent storage locations in sequence until an entire data file is written or read. The present claims, however, define a disk like approach to semiconductor memory operation. The fact that the system of the Burke patent may look to the host system as a disk memory system does not mean that its array is operated in sectors, with headers, etc., as claimed. While sector addressing may be used between a host and the controller, the host does not know or care what type of addressing is being used between the controller and the memory media. In the case of a magnetic disk media, its physical attributes have naturally resulted in sector addressing by the controller. But for a random accessed solid state memory, it is more efficient to address the memory by large files, such as one that is transferred by a DMA (Direct Memory Access) controller. As a general proposition, a memory system controller can manipulate and rearrange storage of data in the semiconductor memory in any number of ways while the controller makes the memory system appear to the host system as a disk drive memory.

Furthermore, with regard to the storage of a header (overhead data) along with user data of individual sectors, it includes auxiliary information being used by the controller to properly and efficiently access particular sectors, given the particular physical characteristics of the memory medium. It is in the nature of semiconductor RAMs, however, that no such auxiliary information is required to access the memory itself.

However, the flash EEPROM system employed in the present invention, unlike typical RAMs, do have memory operations that can benefit from auxiliary information. The provision for making such information available in a header of each sector in the context of a solid state memory is part of the present invention.

An underlying assumption made throughout the Examiner's Action is that it is *inherent* in the system of the cited Burke reference to operate its volatile RAM array with sectors, and thus obvious to include overhead data (headers) in individual sectors. This premise, and thus all the rejections based upon it, is respectfully submitted to be incorrect. Contrary to the position

taken in the Examiner's Action, it is submitted that the fact that Burke's system looks to the host system as a disk drive memory does not compel this conclusion. The alleged inherent Burke disclosure upon which nearly all the grounds of rejection are based does not exist.

Application of the doctrine of "inherency" is not appropriate in this case. As noted by the court in Ethyl Molded Products Company v. Betts Package Inc., 9 U.S.P.Q. 2d 1001, 1032-1033 (E.D. Kentucky, 1988):

> The doctrine of inherency is available only when the prior inherent event can be established as a certainty. That an event may result from a given set of circumstances is not sufficient to establish anticipation. Probabilities are not sufficient . . . A prior inherent event cannot be established based upon speculation, or where a doubt exists.

In this case, the operation of the semiconductor memory of Burke that is found to be "inherent" is not at all certain but rather is a conclusion formed simply from the fact that the memory interfaces to the host system with a sector format. There can be no doubt that this determination lacks the required certainty. It is thus respectfully submitted that all the outstanding rejections based thereon must be withdrawn.

It is also respectfully submitted that the Official Notice of prior art "facts" taken extensively throughout the Examiner's Action is in error. This procedure is proper for facts that are unquestionably well known in the art or generally known but is not proper to establish technical facts that are not well known or which are in esoteric technology. See the M.P.E.P., section 2144.03, Sept. 1995. As discussed below with respect to specific facts attempted to be established in the Examiner's Action by taking Official Notice of them, those facts are far from being generally known. They pertain to quite detailed aspects of computer memory technology. The taking of Official Notice of such facts in submitted to be improper.

Furthermore, it is respectfully submitted that certain of the alleged "facts" are not correct. An example is the assertion that ".. it is known in the art that the information bits in a

group of bit-storing units (called sector) in a magnetic memory device are erasable together as a unit;" (Examiner's Action, p. 10, para. d). But the fact is that sectors of magnetic memories are not individually erased during operation. They are simply written over with new data when required. If there is some existing prior art that describes a magnetic disk system where the sectors are individually erasable as a unit, it should be cited since this is certainly not the common practice. It is definitely not appropriate to take Official Notice of such a fact for the purpose of rejecting claims.

Claims 79-84, 98 and 99

Reconsideration is respectfully requested of the rejection of independent claim 79, and its dependent claims 80-84, 98 and 99, as obvious over a combination of the cited Burke, Yorimoto *et al.* and Satoh *et al.* references, as well as certain facts of which Official Notice is being taken. In rejecting claim 79, the Examiner's Action states the following: "Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to 'emulate' a magnetic disk which has sectors." (Examiner's Action, p. 4.) This is the assumption about Burke which, as discussed in the preceding section, is believed to be in error. Yorimoto *et al.* is then cited as evidence that it would have been obvious to partition Burke's inherent sectors into user data and overhead data portions. Satoh *et al.* is further cited as evidence that it would have been obvious to provide for substitution of a useable sector for an unusable sector of the Yorimoto *et al.* modified Burke inherently sectored memory.

It is respectfully submitted that the basis expressed for the rejection is in error. The claims in this application each define more than the desire to make a semiconductor memory system look on the host system side of the memory controller to be a disk drive. They define a way of configuring and using a semiconductor memory on the memory side of the controller in a way similar to a disk drive. Claim 79 defines a flash EEPROM system with an array that is divided into sectors of cells that are erasable together as a unit. This is not new by itself but is a particular type of

memory which is recited by claims 79-84 to be used to emulate a disk drive. None of the three cited references suggest use of such a type of memory. The only mention of an EEPROM system is by Yorimoto *et al.* but their embodiments appear to be generically described for use with either an EEPROM or a battery backed volatile RAM. Nothing is said by Yorimoto *et al.* of a flash EEPROM system that is operated with sectors of cells that are erasable together as a unit. It is the use of this type of memory that allows the memory itself to be operated very similarly to that of a disk drive, with individual sectors that store both user data and overhead data (a header for the sector). It is the operation of the flash EEPROM memory by the memory controller with the sectored and partitioned characteristics of a disk drive memory that is novel and non-obvious.

The disclosure by Burke of his semiconductor memory system "emulating a rotating magnetic memory device" certainly does not suggest that his controller operates the semiconductor memory in the claimed sectored and partitioned manner. There is nothing "inherent" from the expressed disk emulation that suggests that Burke operates its semiconductor memory in the sectored manner being claimed. What the emulation states is that the controller interfaces with the host computer system as if it is a disk drive but the controller could operate the semiconductor memory in any number of ways. Although Burke discloses operating his semiconductor memory in groups of 64K cells, it appears that his controller interfaces with and operates the semiconductor memory in traditional ways, rather than emulating disk drive memory sectors. One skilled in the art, it is submitted, would therefore not have found it obvious to apply the sector partitioning technique of Yorimoto *et al.* It is not seen how one skilled in the art could have found it obvious to form a combination of such different memory architectures.

It is further not understood what type of block substitution in the Burke system would the disk drive system of Satoh *et al.* have suggested to one ordinarily skilled in the art. Would it be substitution of one of Burke's large 64k groups for another? It is submitted that it would not have been obvious to

apply the disk drive substitution technique of Satoh *et al.* to Burke's memory. But also important is that none of the three references cited against claims 79-84 suggest a sectored flash EEPROM system where the cells of the individual sectors are erasable together, let alone the use of the disk drive techniques of a header (overhead data) and unusable sector substitution to such a defined flash EEPROM sector.

Dependent claims 80 and 81 recite that a sector is replaced because a certain number of cells of the sector are defective. It is believed to be quite unusual, if it has ever occurred in the prior art, for defects in volatile semiconductor RAMs (as in the Burke reference) to be handled by throwing away such a large proportion of a memory, much of which would likely remain good. The rejection of claim 81 is predicated upon Official Notice being taken of certain facts (Examiner's Action, p. 6, first paragraph). It cannot be accepted that the prior art fact there alleged to exist is "notoriously old and well known" but it can be pointed out that defect management prior art has been made of record in this application. It is requested that any further rejection of claim 81 be based upon actual prior art rather than that believed by the Examiner to exist.

With respect to claim 82, the Examiner's Action states that "The size of 512-bytes, which is took (sic.) as a given amount of user data, is of obvious design choice." But the point of this claim is that the flash EEPROM memory is sectored exactly like the disk drive which it emulates. The memory controller does more than just appear to the host computer system to be a disk drive, it operates the flash EEPROM cell array like a disk drive. New claim 144, also dependent upon claim 79, recites that the disk drive and flash EEPROM formats are the same in that each carries substantially the same amount of data.

Claim 83 adds to the combination of claim 79 that the overhead data (header) in the individual flash EEPROM sectors includes the address of the sector in which it resides. This further defines the unique operation of the flash EEPROM system to operate as a disk drive. Claim 84 recites that the overhead data

of a sector includes an error correction code (ECC) that has been calculated from the user data stored in the same sector.

Dependent claims 98 and 99 have been rejected as obvious over the same three references as their parent claim 79, plus some alleged prior art about which Official Notice has been taken. These dependent claims add to the method of claim 79 two techniques for linking the address of a usable sector with an unusable one, in the course of sector substitution. It cannot be accepted that alleged facts a. through f. on page 6 the Examiner's Action ".. are notoriously old and well known in the art of memory patching." Nor can it be accepted that one ordinarily skilled in the art would have been motivated to use this alleged notoriously old prior art in the was suggested in subparagraphs a-d on page 7 of the Examiner's Action. Certain prior art of defect management of flash EEPROM systems has been made of record, and it is suggested that any further rejection of these claims be based upon actual prior art. To the extent that the Examiner's Action is taking Official Notice of some of the facts a.-f. allegedly being true with regard to disk drive memory systems, it can be pointed out again that a feature of the present invention is the operation of a flash EEPROM system by the memory controller as if a disk drive. This is more than making the controller look like a disk drive to the computer system, as the Burke reference says it is doing, but claims 98 and 99 define organizing and operating the flash EEPROM cell array in ways similar to that of a magnetic disk drive memory.

Claims 85-91

Reconsideration of the rejection of claims 85-91 is respectfully requested. These claims stand rejected as obvious over a combination of the Burke and Yorimoto *et al.* references. They are submitted as patentable for the same reasons stated above with respect to this combination of these same references applied to claims 79-84.

Claims 92-97

Independent claim 92 has been rejected as obvious over a combination of the cited Burke and Yorimoto *et al.* references. It is submitted that claim 92 is patentable on the ground that the Burke reference does not implicitly operate, as asserted in the

Examiner's Action, with its memory divided into sectors in the manner claimed. His 64K groups of cells are not intended to emulate disk drive sectors. It is therefore submitted that it would not have been obvious to partition any such groups into user and overhead data portions in accordance with the Yorimoto *et al.* reference, as alleged in the Examiner's Action.

Response is required to the characterizations of the Burke reference that were made in the paragraph bridging pages 8 and 9 of the Examiner's Action. No disclosure of sector addressing signals in the manner claimed is found in the Burke reference. The Burke reference does express a purpose to emulate a disk drive by appearing as a disk drive on the side of its controller that interfaces with the host computer system. But this does not make it implicit, it is submitted, that the semiconductor memory, on an opposite side of the memory controller, be divided into disk like sectors that are erasable together as a unit, contrary to what is alleged in the Examiner's Action. The type of memory disclosed in the Burke reference is made of an array of volatile dynamic RAM cells which are not erased in blocks since such cells lose their charge over time and are periodically refreshed in order to maintain their charge. The Burke system even provides for such refresh (see paragraph bridging pages 11 and 12, for example) in order to prevent their erasure.

Nor does the cited Yorimoto *et al.* reference suggest a semiconductor memory array that is divided into sectors of cells that are erased as a unit. The fact that Yorimoto *et al.* describe using an EEPROM cell array does not necessarily mean that any division of the cells into logical groups results in all cells of a group being erased together as a unit. Some EEPROM systems in the prior art operate like normal RAM systems, without the sector organization defined in claim 92.

It cannot be agreed that Official Notice is appropriately taken of alleged facts (1) through (3) of the first full paragraph of page 9. It is requested, if these rejections are continued, that appropriate prior art references be cited in support of these alleged facts, in order that a specific situation is presented to which a response can be made.

The analysis given on pages 9-11 of the Examiner's Action of the obviousness of claim 92 over the cited Burke and Yorimoto *et al.* references is submitted to be based upon erroneous factual assumptions. The fact that Burke looks to the host system as a disk drive does not make it necessary for his controller to actually operate the volatile RAM memory with the same sector characteristics as a disk drive, because that is such a different way than RAM memory is normally operated. No part of Burke's dynamic RAM cell array is erasable as a unit. To say that such a memory array is, in addition to not being described by Burke, erased in sectors is contrary to the nature of the memory cells being used. There is also no requirement that appears to exist in the Burke system to store overhead information as part of any such sector. What Burke's controller seems to do well, at least in his description, is to appear to the host system to be a disk drive memory while operating the dynamic RAM array in accordance with its particular characteristics. The fact that Burke describes emulating a disk drive does not necessarily mean, nor does it suggest, that his semiconductor array is operated with disk like attributes; namely, being divided into the claimed sectors, with overhead data (headers) stored in the individual sectors to which they pertain, usable sectors being swapped for unusable sectors, etc.

Further, the Yorimoto *et al.* reference does not suggest partitioning its EEPROM cell array into sectors that simulate those of a disk memory, as alleged in the Examiner's Action. No discussion has been noted in the Yorimoto *et al.* reference of erasing the cells within such sectors as a unit. It could be that Yorimoto *et al.* contemplated erasing the entire memory at once, which was quite common a few years ago. What is being claimed in claim 92 of the present application is a flash EEPROM cell array that is operated by its controller with characteristics that are like that of a disk drive. The suggestion of such a structure is simply not made by either of the cited Burke or Yorimoto *et al.* references.

Additionally, claim 92 has been amended to make clearer that the memory system operates to read the overhead data (header)

of an addressed sector before user data is either written to or read from the user data portion of the sector. This is another feature that departs from the usual operation of a semiconductor memory to make the flash EEPROM system operate as a disk drive memory system, and is not disclosed in either of the Burke or Yorimoto references. It is believed to be a significant departure from normal semiconductor RAM system operation to divide a memory array into sectors that individually have user data and overhead data portions, and then to read the overhead data from an addressed sector before user data is read from or written to the addressed sector. It is especially nonobvious to read a semiconductor memory sector's overhead data (header) before writing user data to that sector.

The Examiner's Action, however, in paragraphs g. and h. of page 10, paraphrase this claimed feature as prior art of which Official Notice is being taken. It is respectfully submitted that this is not a proper analysis of what one skilled in the art would have been led, prior to April 13, 1989, to find obvious. Rather, these statements merely allege obviousness without providing any factual basis to support the allegation. For example, what would have led one of ordinary skill in the art to recognize a need to validate the sector by first reading the overhead data from that sector? It is respectfully submitted that it is not enough to merely state, in a conclusionary manner and without reference to evidence of prior art, that a claimed difference over the prior art is obvious.

Claims 93-97, dependent upon claim 92, stand rejected as does claim 92 but with the Nozawa *et al.* patent additionally used to form obviousness rejections. But Nozawa *et al.* describe a disk drive memory system and do not, it is respectfully submitted, suggest ways to modify the Burke memory cell array to meet the terms of the claims. Since the Burke system does not operate his dynamic RAM cell array with disk like sector characteristics, as claimed, it is submitted that Nozawa *et al.* would not have suggested to one of ordinary skill in the art any modification of the Burke reference that could have resulted in the system defined by any of claims 93-97. Particularly, it is submitted that one

ordinarily skilled in the art would not have considered it obvious to use a disk drive sector pointing technique for substituting usable sectors for unusable sectors in the system of Burke that operates its dynamic RAM cell array without disk like sectors.

Claims 116-127

Independent claim 116 also stands rejected on the ground of obviousness over the cited Burke and Yorimoto *et al.* references. Claim 116 is similar in structure to claim 92 but is more specific in reciting flash EEPROM sector substitution. Claim 116 is also being amended to make clear that the addressed sector has its overhead data read before user data is either read from or written into that sector. Dependent claims 117, 121 and 124 stand rejected over the Burke and Yorimoto *et al.* patents, as with parent claim 116, plus the Nozawa *et al.* patent. Claim 116 and its dependent claims 117-127 are submitted to be patentable for the same reasons given above in support of the patentability of claim 92 and its dependent claims 93-97. The taking of Official Notice of certain prior art "facts" to reject claims 116-127 is submitted to be improper.

New Claims 128-143

New independent claim 128 includes use of a flash EEPROM cell array divided into separately erasable sectors that are erasable together as a unit. Overhead data is stored in each sector. A write operation is conducted by first reading overhead data from the addressed sectors and thereafter writing the user data and other overhead data. A read operation includes reading overhead data of a sector before reading its user data. These elements of novelty, most of which are extensively discussed above with respect to other claims, are submitted to render claim 128 patentable. New claims 129-143 add other novel elements, most of which have also been discussed above with respect to the prior art.

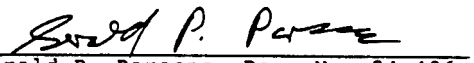
Conclusion

For the reasons stated above, it is submitted that the present application is in condition for allowance. However, should

the Examiner have any further matters that need to be resolved, the undersigned attorney would appreciate a telephone call.

Dated: June 7, 1996

Respectfully submitted,



Gerald P. Parsons, Reg. No. 24,486
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San Francisco, CA 94111-4121
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Facsimile: (415) 362-5418

Atty. Docket: HARI-0606

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
ELIYAHOU HARARI et al.
Serial No.: 08/174,768
Filed: December 29, 1993
For: FLASH EEPROM SYSTEM

Group Art Unit: 2413
Examiner: L. Hua

San Francisco, California

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Amendments Commissioner of Patents and Trademarks, Washington, D.C. 20231 on June 7, 1996.

Brenda J. Dolly

Brenda J. Dolly 6/07/96
Signature Date

AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is an amendment in the captioned application. A check in the amount of $78.00 is enclosed to cover the fee for filing an additional claim.

A three-month extension of time in which to respond to the outstanding Office Action is hereby requested and a check in the amount of $900.00 is enclosed to cover the fee.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: June 7, 1996

Gerald P. Parsons, Reg. No. 24,486
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Atty. Docket: HARI-0606


16

220. '76

2413
#16
C.D.
7/19/96

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
ELIYAHOU HARARI et al.)
Serial No.: 08/174,768)
Filed: December 29, 1993)
For: FLASH EEPROM SYSTEM)

Group Art Unit: 2413
Examiner: L. Hua

San Francisco, California

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING UNDER 37 CFR 1.10

I hereby certify that this patent application transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" Mailing Label Number EM016644649US addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on June 28, 1996.

Name: Brenda J. Dolly
Signature 6/28/96 Date

SIXTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

The following Form 1449 and copies of each cited document is being filed herewith as a Sixth Supplemental Information Disclosure Statement. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, is respectfully requested.

The required fee of $220.00 is being filed herewith. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: June 28, 1996

Gerald P. Parsons, Reg. No. 24,486
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Atty. Docket: HARI-0606

FORM PTO1449 (REV. 8-83) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
HARI-0606	08/174,768
APPLICANT Eliyahou Harari	
FILED December 29, 1993	**GROUP** 2413

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A17	4 0 9 3 9 8 5	6/1978	Das	395	185.02	
	A18	4 2 7 9 0 2 4	7/1981	Schrenk	365	185.22	
	A19	4 6 1 6 3 1 1	10/1986	Sato	395	416	
	A20	4 7 1 8 0 4 1	1/1988	Baglee et al.	365	185.22	
	A21	4 7 8 5 4 2 5	11/1988	Lavelle	365	52	
	A22	4 8 0 0 5 2 0	1/1989	Iijima	235	382	
	A23	4 8 8 7 2 3 4	12/1989	Iijima	395	497.04	
	A24	4 9 4 9 2 4 0	8/1990	Iijima	395	600	
	A25	5 0 5 3 9 9 0	10/1991	Kreifels et al.	395	430	
	A26	5 0 7 0 4 7 4	12/1991	Tuma et al.	395	416	
	A27	5 0 9 5 3 4 4	3/1992	Harari	365	185.03x	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
	B10	58 - 2 1 5 7 9 4	12/1983	Japan	—	—	YES
	B11	58 - 2 1 5 7 9 5	12/1983	Japan	—	—	YES
	B12	59 - 1 6 2 6 9 5	9/1984	Japan	—	—	YES
	B13	60 - 2 1 2 9 0 0	10/1985	Japan	—	—	YES
	B14	62 - 2 8 3 4 9 6	12/1987	Japan	—	—	YES
	B15	60 - 0 7 6 0 9 7	4/1985	Japan	—	—	Abstr

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

	C5	Lucero et al., "A 16 kbit Smart 5 V-only EEPROM with Redundancy," *IEEE Journal of Solid-State Circuits*, vol. SC-18, no. 5, pps. 539-543 (October 1983)
	C6	Torelli et al., "An improved method for programming a word-eras-able EEPROM," *Alta Frequenza*, vol. 52, no. 6, pps. 487-494 (Nov.-Dec. 1983)

EXAMINER	DATE CONSIDERED
Ly V. Hua	8/16/96

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI-0606	SERIAL NO. 08/174,768
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT Eliyahou Harari	
		FILED December 29, 1993	GROUP 2413

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
LDL	B16	59 - 4 5 6 9 5	3/1984	Japan	—	—	Abstr.
LDL	B19	61 - 9 6 5 9 8	5/1986	Japan	—	—	Abstr.
LDL	B23	62 - 2 8 3 4 9 7	12/1987	Japan	—	—	Abstr.
LDL	B24	63 - 1 8 3 7 0 0	7/1988	Japan	—	—	Abstr.

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

LDL	C7	Data Sheet: "27F256 256K(32K x 8) CMOS Flash Memory," *Intel Corporation*, pps. 1-24 (May 1988)
LDL	C8	Preliminary Data Sheet, "48F512 512K Flash EEPROM," *SEEQ Technology, Incorporated*, pps. 2-1 thru 2-12 (October 1988)
LDL	C9	Advanced Data Sheet, "48F010 1024K Flash EEPROM," *SEEQ Technology, Incorporated*, pps. 2-13 thru 2-24 (October 1988)
LDL	C10	Lai, Robert S., *Writing MS-DOS Device Drivers, The Waite Group, Inc.*, September 1987, pp. i-xi and 235-319

EXAMINER	DATE CONSIDERED
Ly V. Hua	8/16/96

* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to

08/174,768

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO
08/174,768	12/29/93	HARARI	E HARI0606

EXAMINER	ART UNIT	PAPER NUMBER
HUA, L	2413	17

24M1/0820

GERALD P. PARSONS
MAJESTIC, PARSONS, SIEBERT & HSUE
FOUR EMBARCADERO CENTER, SUITE 1450
SAN FRANCISCO, CA 94111-4121

DATE MAILED: 08/20/96

NOTICE OF ALLOWABILITY

PART I.

1 ☒ This communication is responsive to Applicant's correspondence filed on June 10 and 28, 1996

2 ☒ All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.

3 ☒ The allowed claims are 79-99 and 116-144

4 ☐ The drawings filed on _____ are acceptable.

5 ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [_] been received. [_] not been received [ ] been filed in parent application Serial No. _____ filed on _____

6. ☐ Note the attached Examiner's Amendment

7. ☐ Note the attached Examiner Interview Summary Record, PTOL-413.

8 ☐ Note the attached Examiner's Statement of Reasons for Allowance.

9 ☐ Note the attached NOTICE OF REFERENCES CITED, PTO-892.

10 ☒ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

1 ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

2 ☒ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER

a ☒ Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No 8 CORRECTION IS REQUIRED

b ☐ The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED

c ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED

d ☒ Formal drawings are now REQUIRED

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:

- Examiner's Amendment
- Examiner Interview Summary Record, PTOL-413
- Reasons for Allowance
- Notice of References Cited, PTO-892
- Information Disclosure Citation, PTO-1449
- Notice of Informal Application, PTO-152
- Notice re Patent Drawings, PTO-948
- Listing of Bonded Draftsmen
- Other

ROBERT W. BEAUSOLIEL, JR.
SUPERVISORY PATENT EXAMINER
GROUP 2400

PTO-37 (REV 4-89) •

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: Box ISSUE FEE
COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

☐ Note attached communication from the Examiner
☐ This notice is issued in view of applicant's communication filed _____

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
First Named Applicant				

TITLE OF INVENTION

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE

THE APPLICATION IDENTIFIES ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY Status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the patent and Trademark Office of the change in status, or
B. If the Status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:
A. Pay FEE DUE shown above, or
B. File verified statement of Small Entity Status before, or with, pay of 1/2 the FEE DUE shown above.

II. Part B of this notice should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B should be completed and returned. If you are charging the ISSUE FEE to your deposit account, Part C of this notice should also be completed and returned.

III. All communications regarding this application must give series code (or filing date), serial number and batch number. Please direct all communication prior to issuance to Box ISSUE FEE unless advised to contrary.

*IMPORTANT REMINDER: **Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
ELIYAHOU HARARI et al.	Group Art Unit: 2413
Serial No.: 08/174,768	Examiner: L. Hua
Filed: December 29, 1993	Attention: Official Draftsman
For: FLASH EEPROM SYSTEM	San Francisco, California

Box Issue Fee
Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Issue Fee, Commissioner of Patents and Trademarks, Washington, D.C. 20231 on October 8, 1996.

Brenda J. Dolly
Signature Oct. 8, 1996
Date

TRANSMITTAL OF FORMAL DRAWINGS

Sir:

Responsive to the Notice of Allowability mailed August 20, 1996, requiring submission of corrected formal drawings in the above-referenced application, please substitute the attached formal drawings, comprising five (5) sheets, for the informal drawings presently of record.

Respectfully submitted,

Dated: October 8, 1996

Philip Yau, Reg. No. 32,892
MAJESTIC, PARSONS, SIEBERT & HSUE
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106
Telephone: (415) 362-5556
Facsimile: (415) 362-5418

Atty. Docket: HARI.006US6

5602987

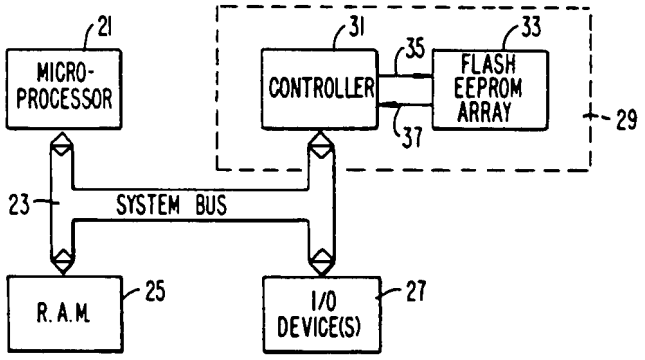


FIG._1A.

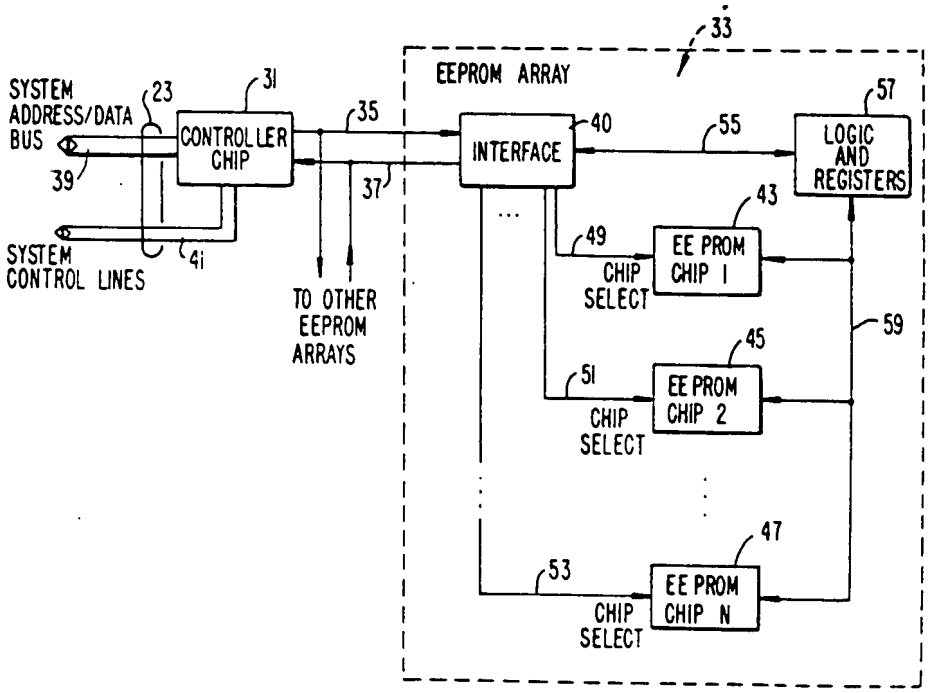


FIG._1B.

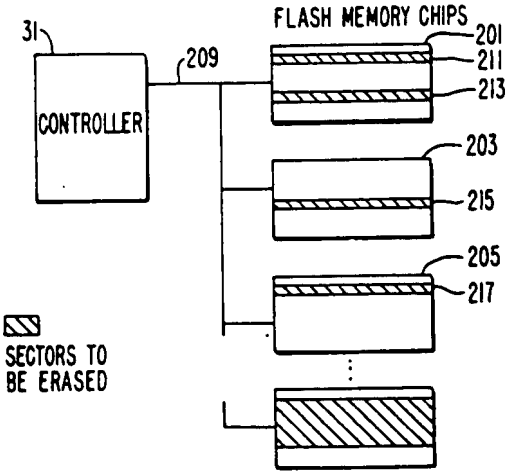


FIG._2.

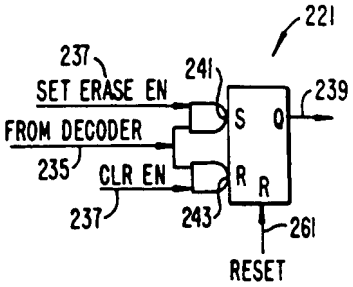


FIG._3B.

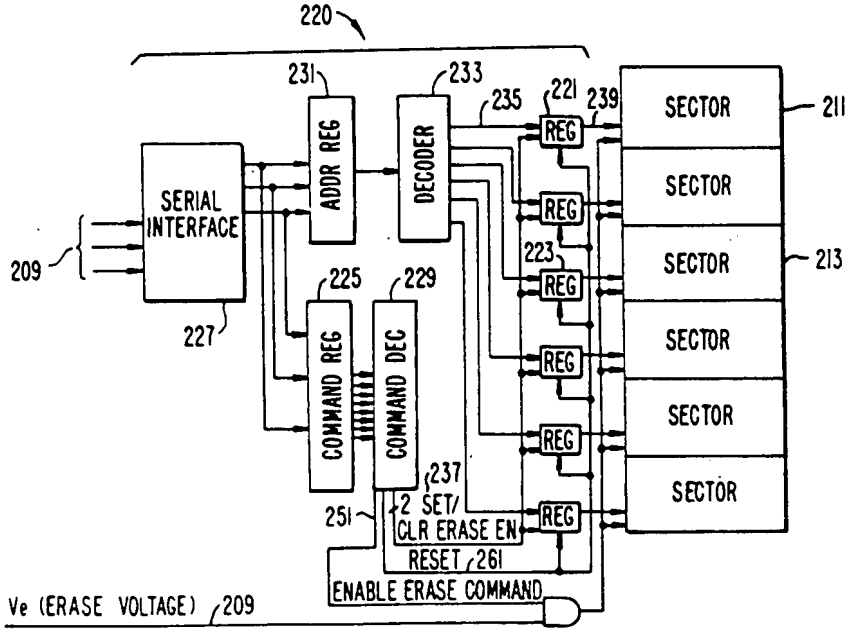


FIG._3A.

WAFER SCALE INTEGRATION

YUKUN HSIA 謝詒昆

UNIVERSITY OF SANTA CLARA
SANTA CLARA, CA. 95053

MICROPROCESSOR DIVISION
FAIRCHILD/SCHLUMBERGER
450 NATIONAL AVENUE
MOUNTAIN VIEW, CA. 94043

07 JUNE, 1984

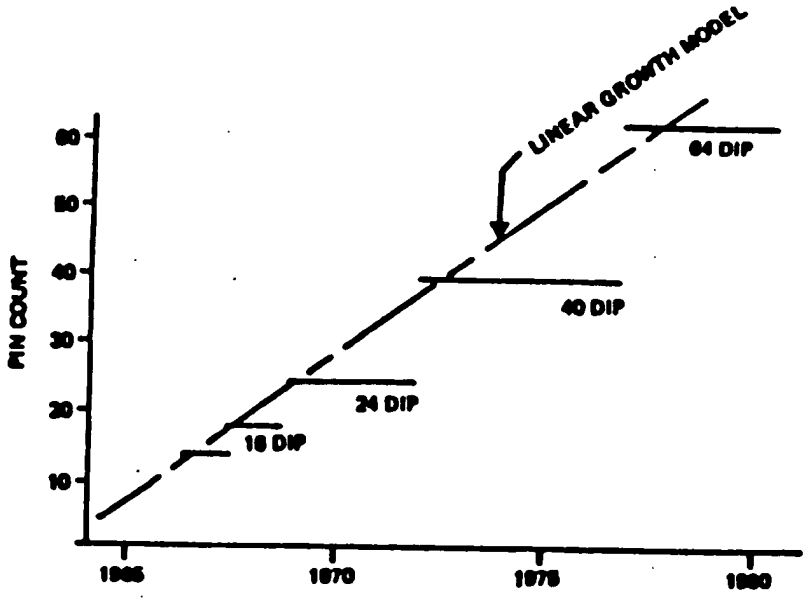
INTEGRATED CIRCUIT TECHNOLOGY

TECHNOLOGY	GATES/CHIP	FUNCTION
SSI	1-30	GATES, FLIP-FLOPS
MSI	30-300	COUNTERS, 4 BIT ADDERS
LSI	300-3K	ALUS, MICROPROCESSORS
VLSI	3K-30K	MULTIPLIERS, A/D CONVERTERS
VHSIC	>30K	FFT'S, COMPLETE COMPUTERS

E. Swartzlander, "VLSI Architecture" from VLSI, Editor: D. F. Barbe, Springer-Verlag, 1980.

PACKAGE PINOUT CONSTRAINTS ON VLSI

(COMMERCIAL DIP'S THROUGH THE YEARS) *

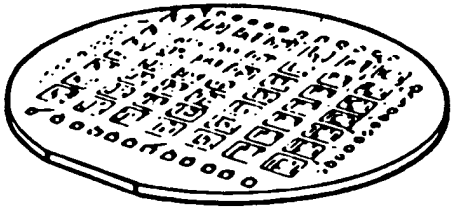


LEX08542

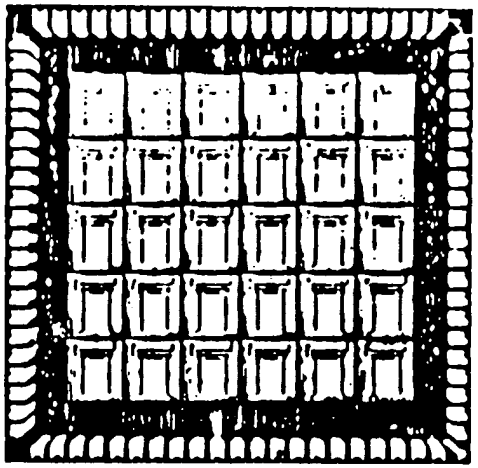
* E. SWARTZLANDER, "VLSI", ED. D. F. BARBE, 1980

AWSI PACKS MORE COMPONENTS AND FUNCTIONS INTO A GIVEN VOLUME

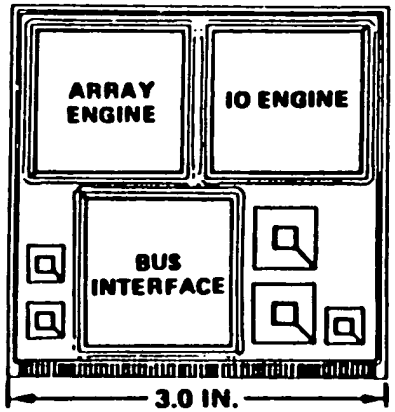
AWSI



SILICON WAFER
MANY INTERCONNECTED CIRCUITS

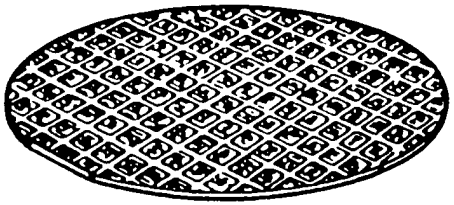


MOUNTED IN
WAFER CARRIER PACKAGE



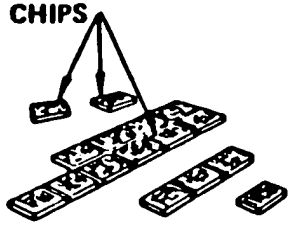
TOTAL SYSTEM OF
RECONFIGURABLE CIRCUITS

LSI

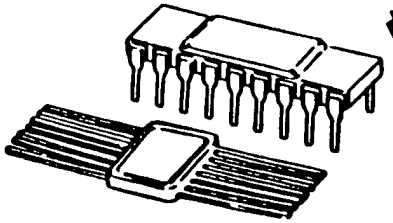


SILICON WAFER
MANY ISOLATED IDENTICAL CHIPS

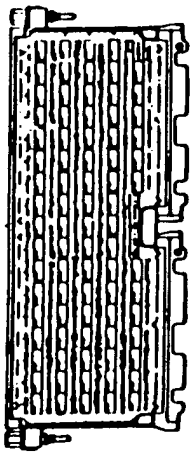
REJECTED CHIPS



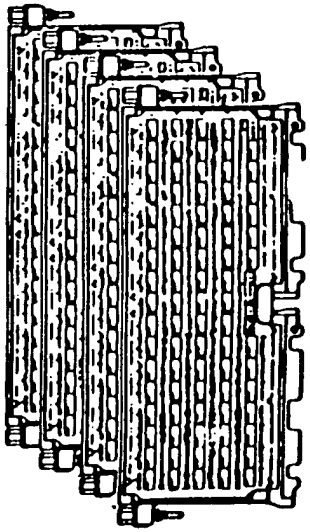
SEPARATE CHIPS



PACKAGED GOOD CHIPS



PACKAGES
MOUNTED ON
CIRCUIT BOARDS



AN ASSEMBLY OF
ELECTRONIC CIRCUITS

LEX08543

NOTABLE WAFER SCALE INTEGRATION EFFORTS

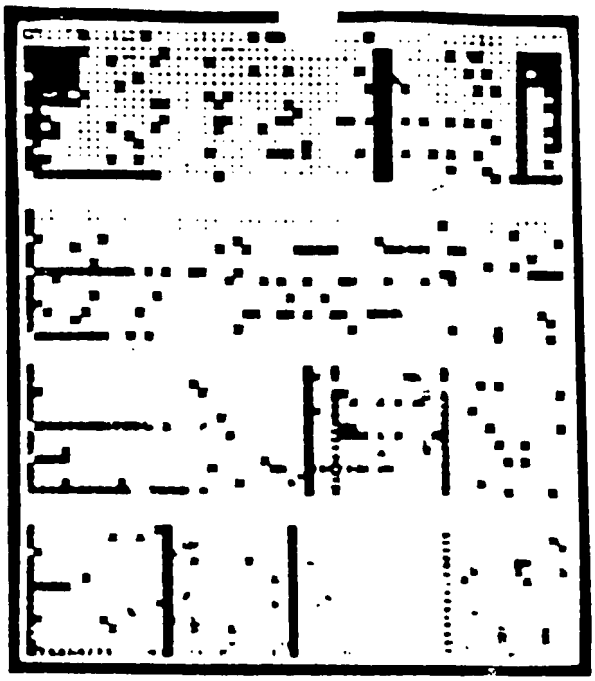
- DISCRETIONARY WIRING
- PAD RELOCATION
- PROGRAMMABLE LINKS
- FULL-WAFER MOS MEMORIES
- ADAPTIVE WSI
- WAFER SCALE SYSTOLIC PROCESSOR
- FULL WAFER CPU (TRILOGY)

LEX08544

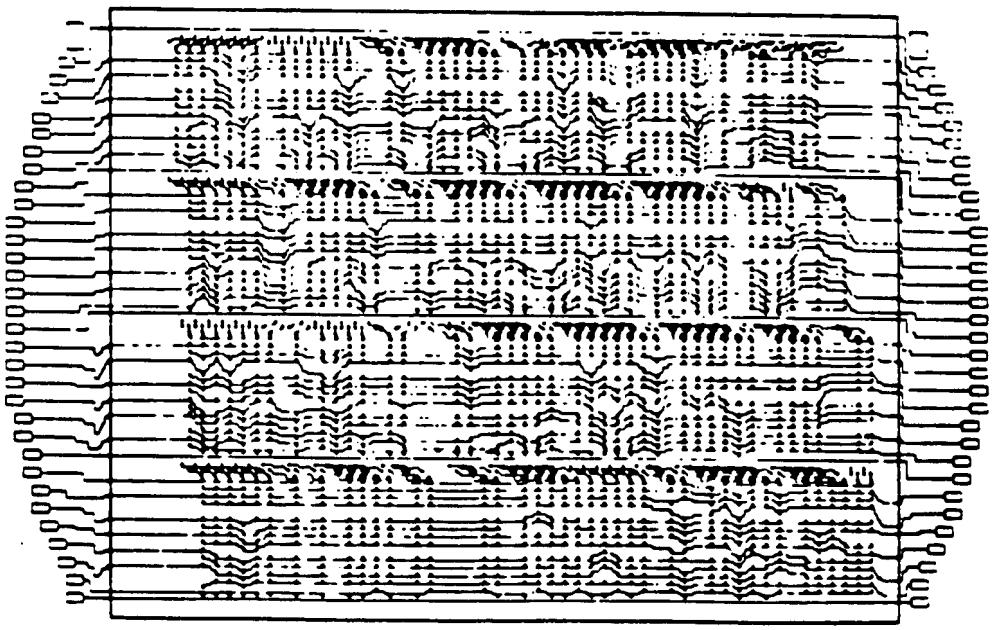
● DISCRETIONARY .ING

ACTIVE MEMORY
SLICE MAP

CELL YIELD=87.4%
WORD YIELD=69.5%



(a)



(b)

(a) Map of memory slice showing bad (dark) and good cells. (b) Discretionary mask drawing for second-level metalization of memory slice.

- PAD RELOCATION

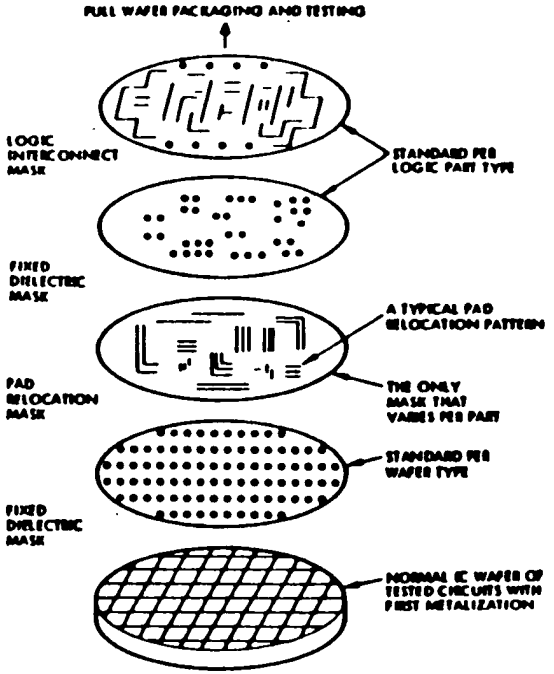
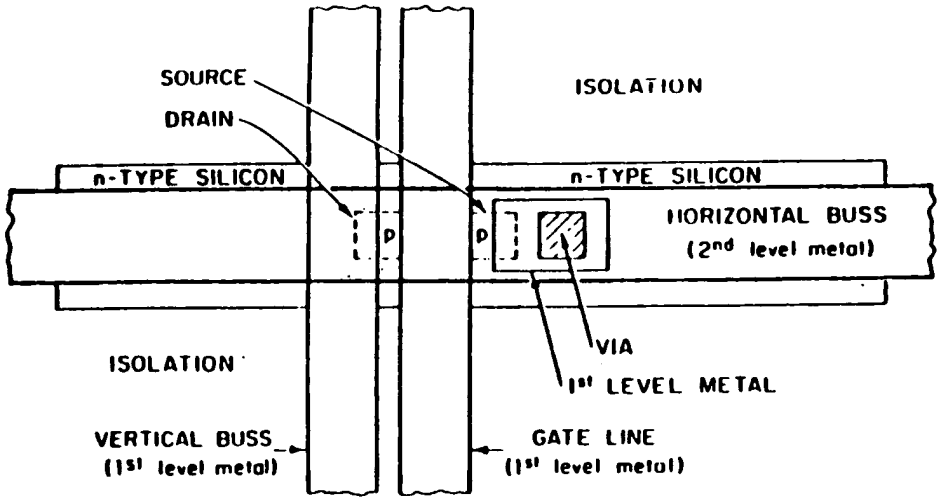
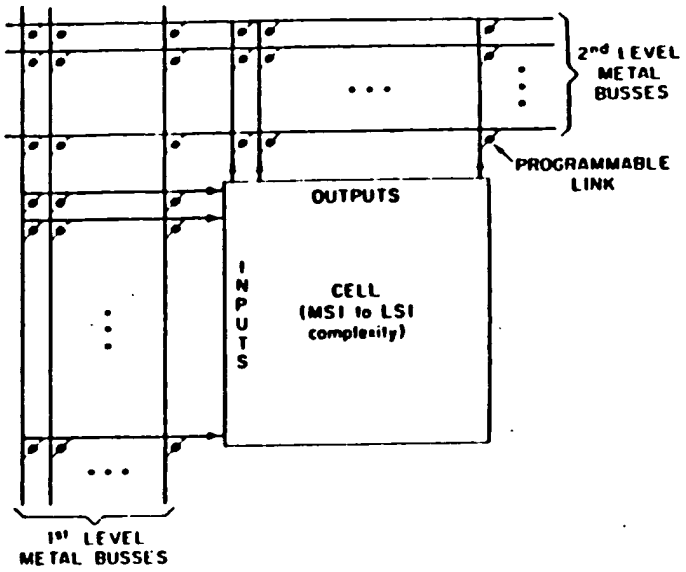


Fig. 1. Four masks required for multilevel interconnect processing on an IC wafer. Only the pad relocation mask is customary and its usage is increased by the technique described here.



NONVOLATILE PROGRAMMABLE LINK

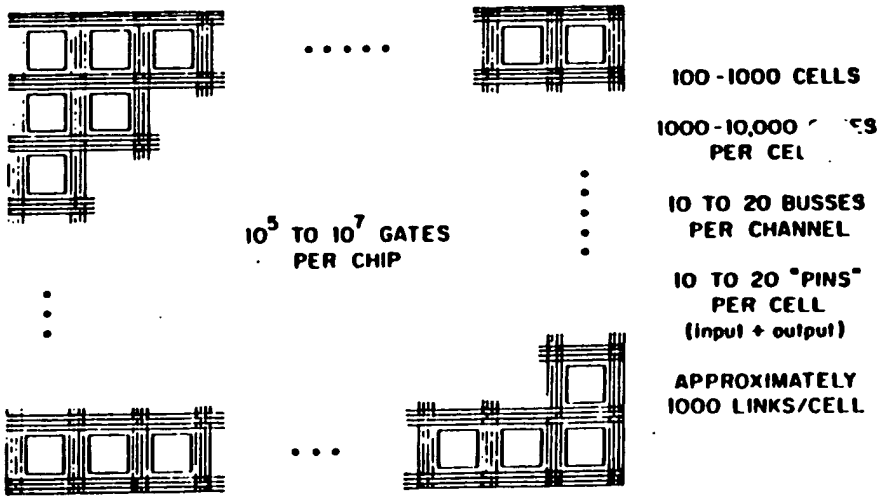


CELL, BUSSES AND PROGRAMMABLE LINKS

On the Use of Nonvolatile Programmable Links for Restructurable VLSI

J. I. Raffel

CALTECH CONFERENCE ON VLSI, January 1979



RESTRUCTURABLE VLSI USING
NONVOLATILE PROGRAMMABLE LINKS

A 1-Mbit Full-Wafer MOS RAM

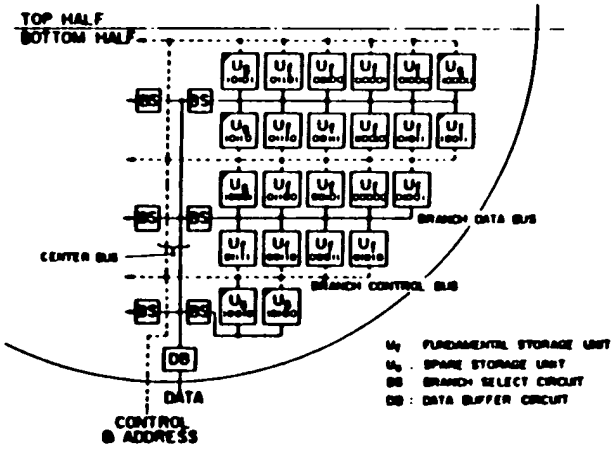


Fig. 1. 1-Mbit wafer RAM block diagram.

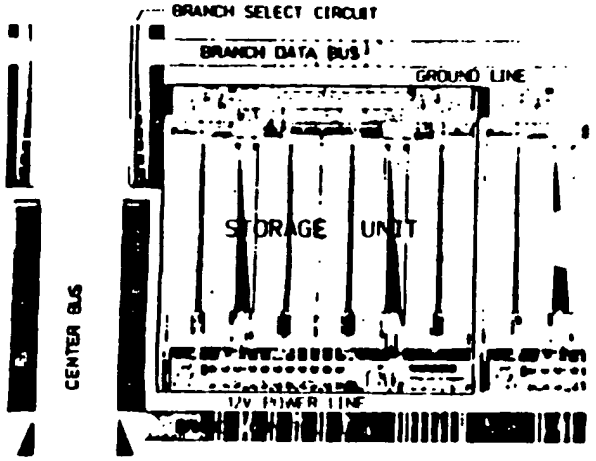


Fig. 2. Photomicrograph of 20-kbit storage units, connected buses, and power supply lines.

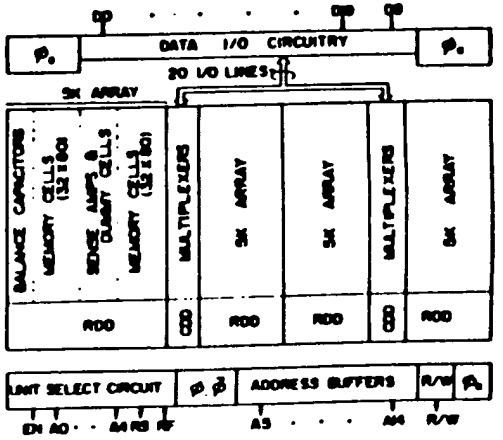
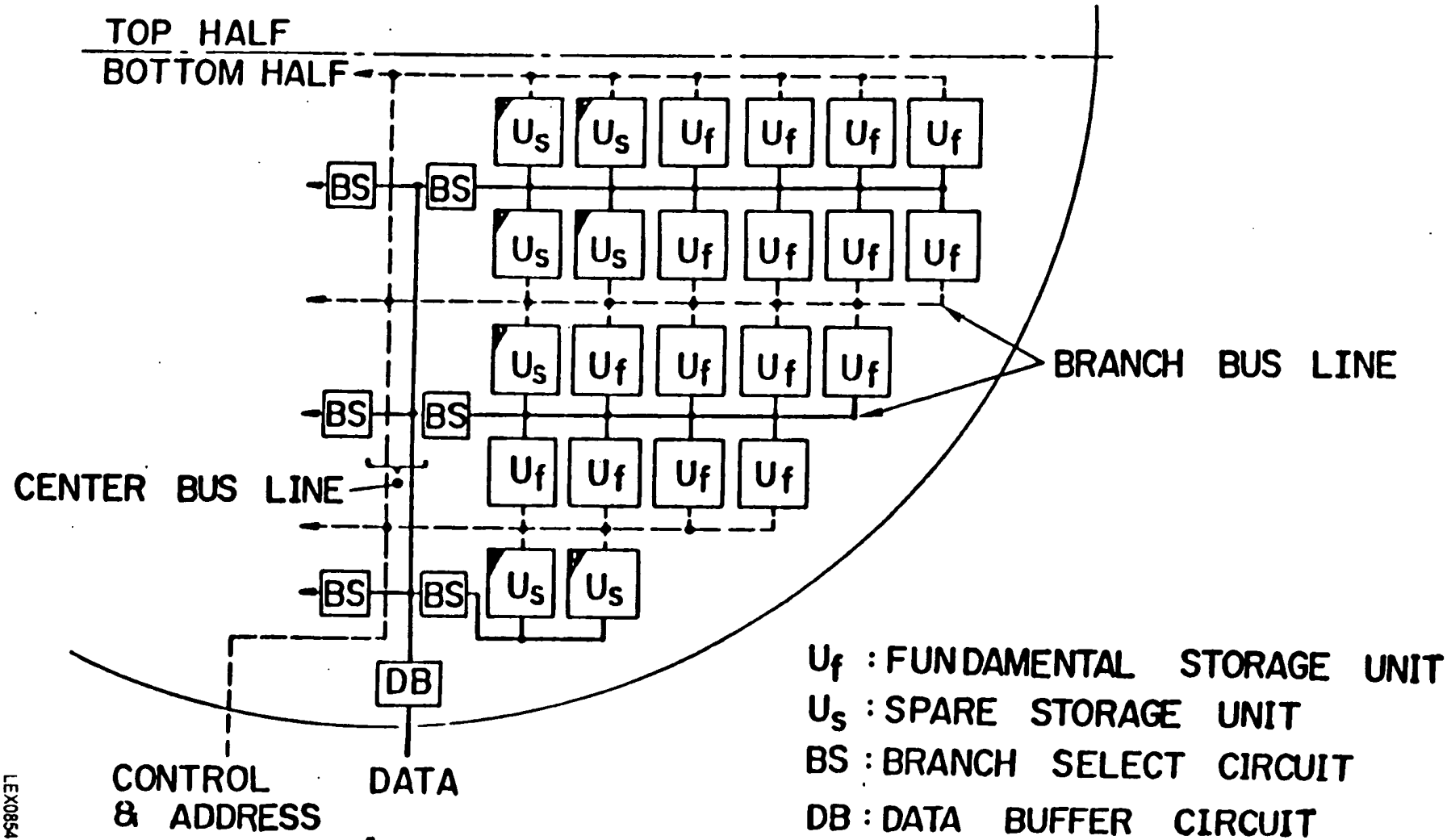


Fig. 3. 20-kbit storage unit block diagram.

LEX08548

SLIDE 1* 1 Mb Full Wafer MOS RAM Blockdiagram

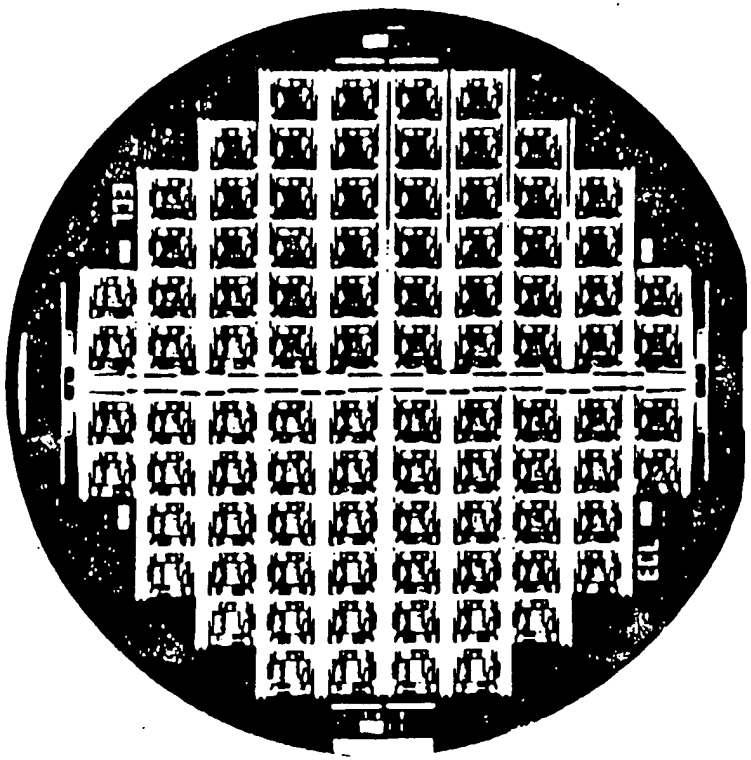


U_f : FUNDAMENTAL STORAGE UNIT
U_s : SPARE STORAGE UNIT
BS : BRANCH SELECT CIRCUIT
DB : DATA BUFFER CIRCUIT

LEX0849

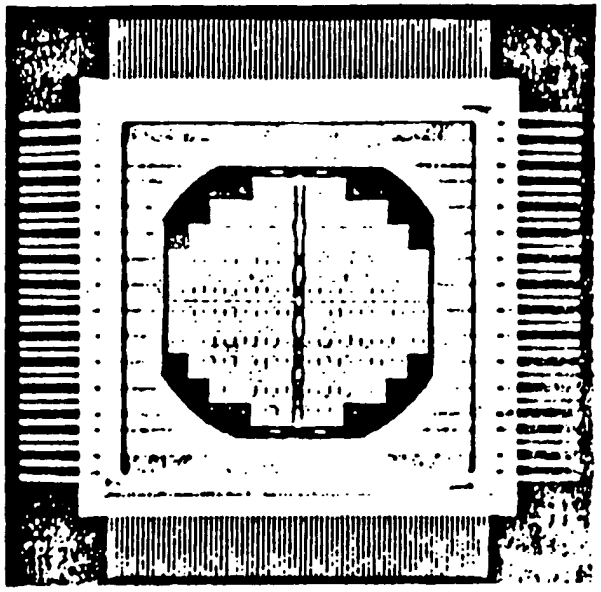
*COURTESY Y. EGAWA,
ALSO Y. EGAWA, ET AL, IEEE ISSCC TECH. DIGEST, p. 18-19, FEB. 1979

ONE MEGABIT RAM*



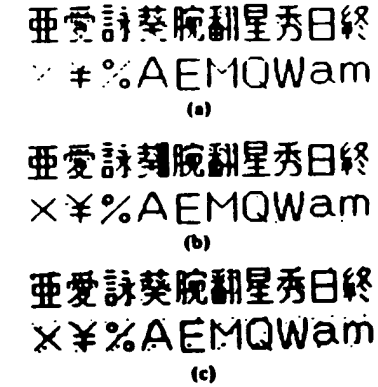
*COURTESY Y. EGAWA,
ALSO Y. EGAWA, ET AL, IEEE ISSCC TECH. DIGEST, p. 18-19, Feb. 1979

LEX08550



1-Mbit full-wafer RAM mounted on a specially designed quad in-line ceramic package.

A 4-Mbit Full-Wafer ROM

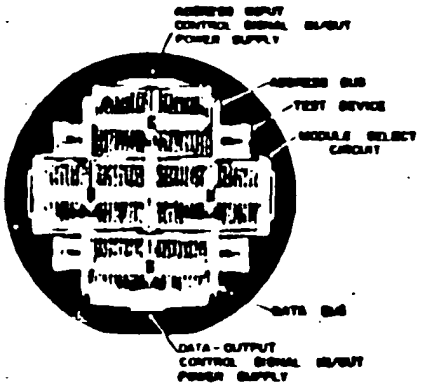


(a)

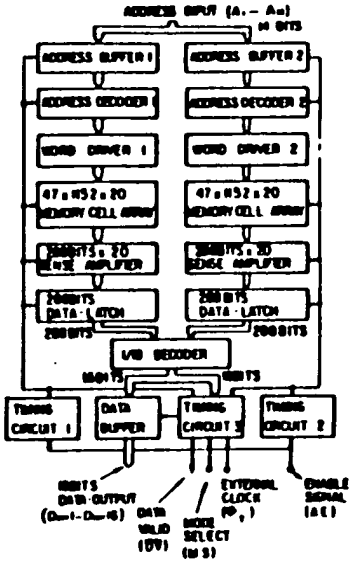
(b)

(c)

Example of output characters. (a) is a duplicated output of (b) and (c). Spot errors in (b) and (c) are all eliminated in (a).



Photograph of a 4-Mbit full-wafer ROM on a 3-in silicon wafer. Four modules are laid out in a rhombus form to save space on a circular wafer. Module-select circuits and test devices are located at the periphery of the wafer.



Block diagram of a module. Memory-cell arrays and principal circuits are duplicated. If address signals and an enable signal are supplied $A1$ to $A14$ and $\overline{AE}$, output data and a data-valid signal are output from $D_{out}1$ to $D_{out}16$ and $\overline{DV}$, synchronized with the external clock ϕ_T.

YUKUN HSIA
GARETH C. C. CHANG
AND F. DENNIS ERWIN

ADAPTIVE WAFER SCALE INTEGRATION

PRESENTED AT THE 1979 INTERNATIONAL CONFERENCE
ON SOLID STATE DEVICES

AUGUST 27-19, 1979, TOKYO, JAPAN

ADAPTIVE WAFER SCALE INTEGRATION

- PRINCIPALLY A SYSTEM INTERCONNECT

  BASED ON IN-SITU ALTERABLE INTERCONNECTIONS WITH STORAGE NONVOLATILITY TO MAINTAIN INTER-CONNECT CONFIGURATION

- LEADS TO

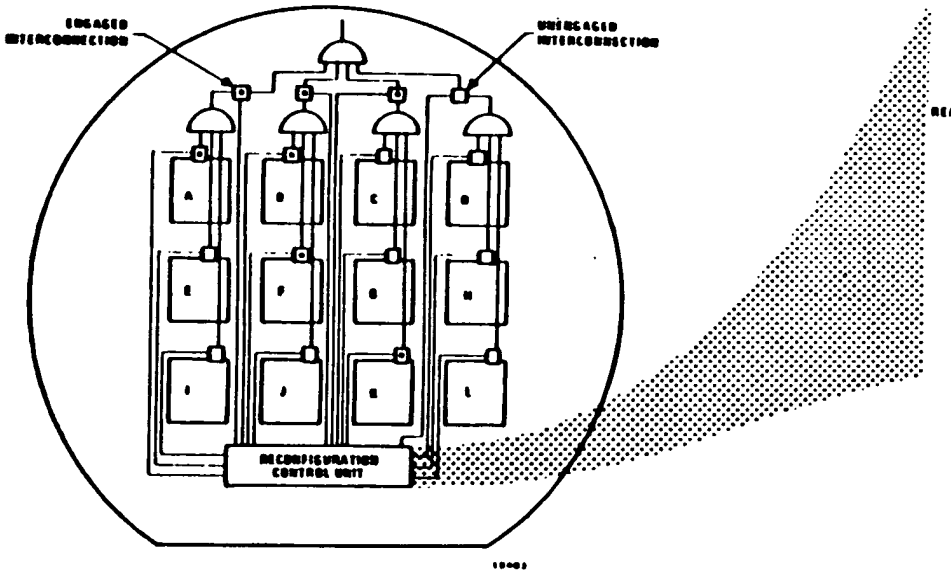
  ADAPTIVITY AND RECONFIGURABILITY IN ELECTRONIC SYSTEMS

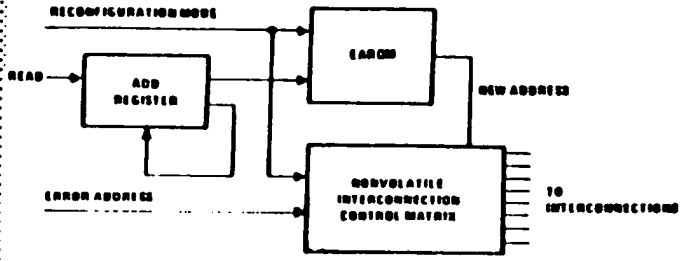
  SELF-ORGANIZING MACHINES

- INCIDENTALLY ALSO A WAFER SCALE INTEGRATION SEMICONDUCTOR TECHNOLOGY

LEX08554

RECONFIGURATION THROUGH WAFER LEVEL INTERCONNECT





MECHANIZATION OF SELF REPAIRING PROCESSOR/MEMORY INTERCONNECTION SYSTEM

- APPLICABLE TO –
  - RECONFIGURABLE MASS MEMORY
  - RECONFIGURABLE LOGIC
  - SELF-REPAIRING MACHINES

LEX08555

AN IN-SITU ALTERNABLE INTERCONNECT FORMS THE BASIS OF AWSI

- RECONFIGURATION
- SELF-REPAIRING REDUNDANCY FOR RELIABILITY
- WAFER SCALE INTEGRATION

MNOS STORAGE WITH AWSI LEADS TO SEMICONDUCTOR MASS MEMORY APPLICATION

- STORAGE NON-VOLATILITY
- LOW OPERATING POWER

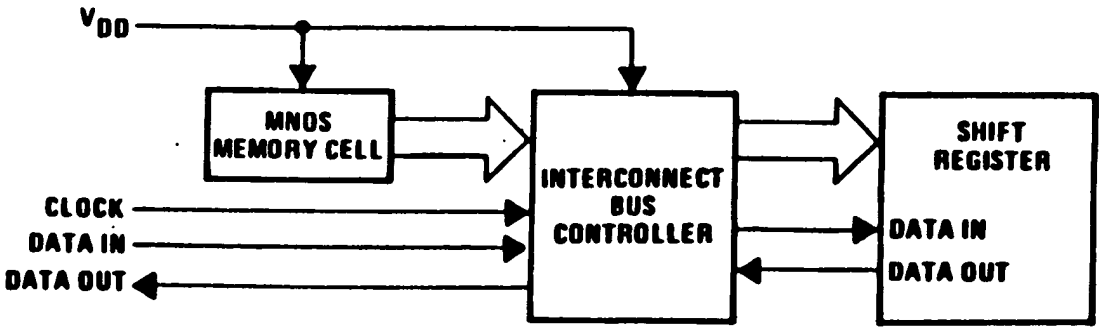
LEX08556

- THE MASS MEMORY IS THE FIRST PRODUCT APPLICATION OF ADAPTIVE WATER SCALE INTEGRATION (AWSI)

- EXPERIMENTAL EFFORTS TOWARD DEVELOPMENT OF THE MASS MEMORY ARE DISCUSSED

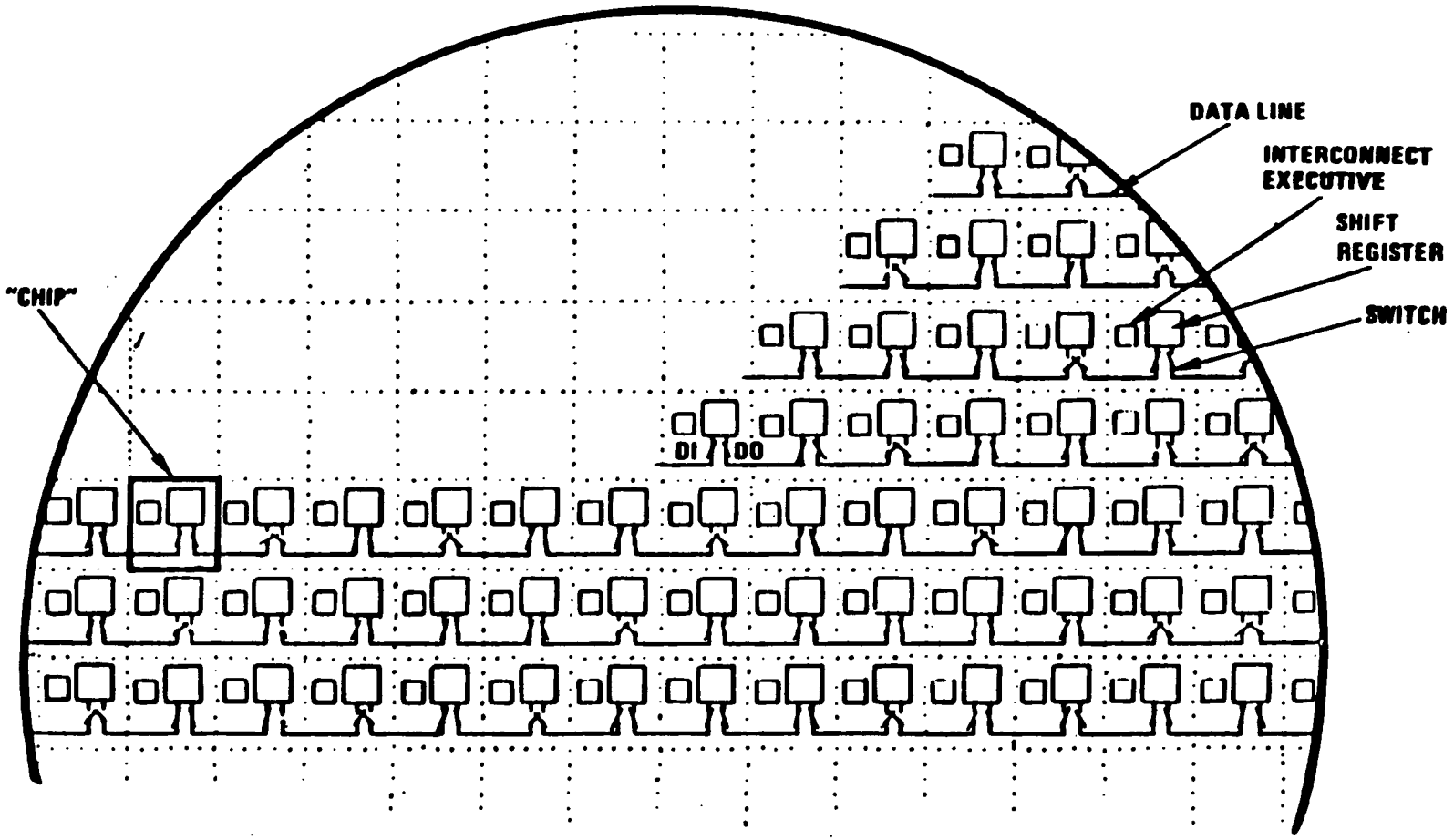
ADAPTIVE WAFER SCALE INTEGRATION

USE OF AWSI TO INTERCONNECT A SHIFT REGISTER STRING

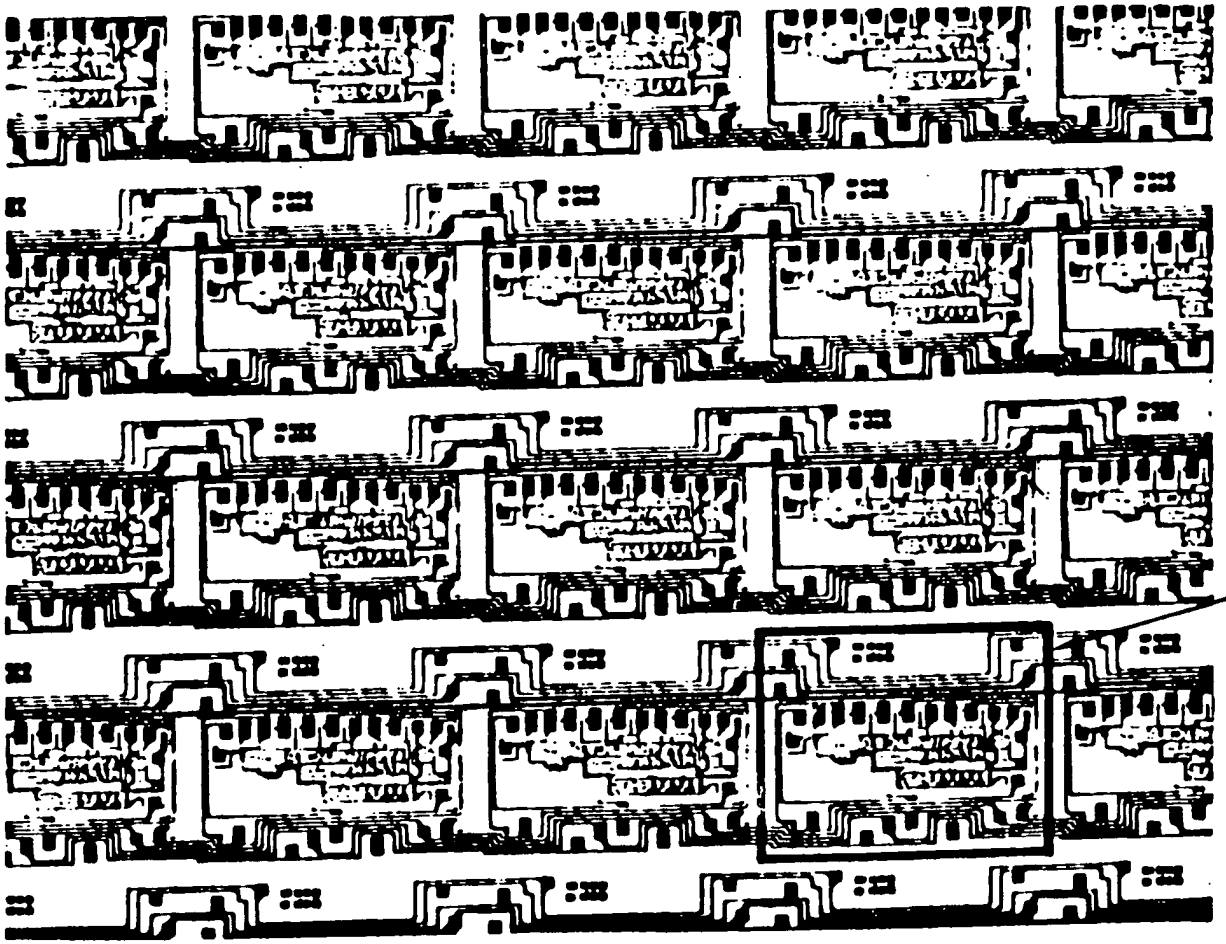


LEX08558

DATA PATH ORGANIZATION OF SHIFT REGISTER STRINGS ON A WAFER

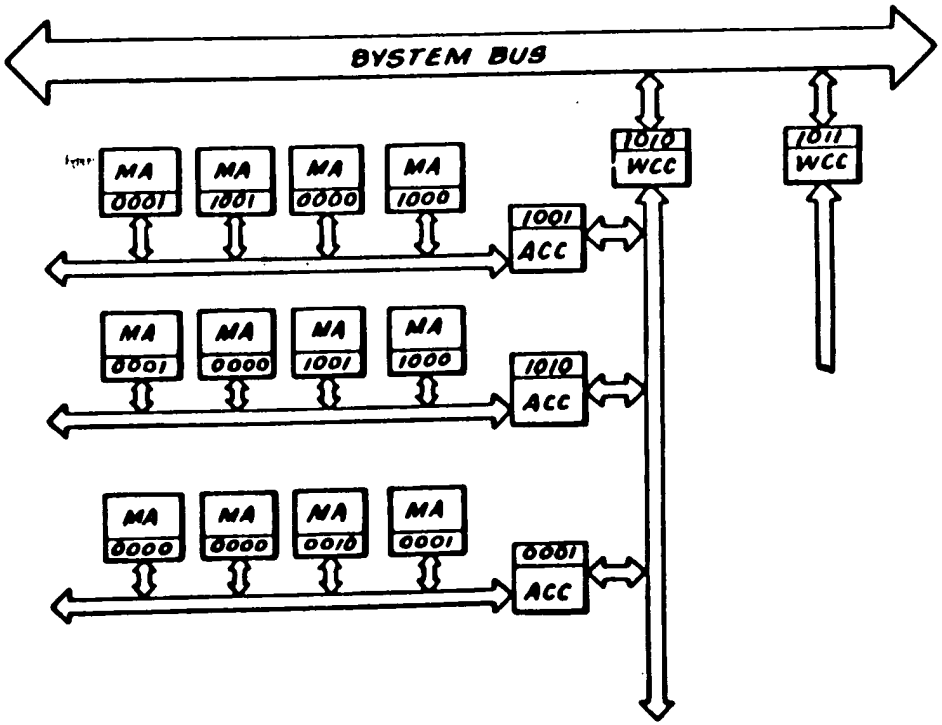


METAL OVERLAY PATTERN
FOR SHIFT REGISTER STRING ON A WAFER



LEX08560

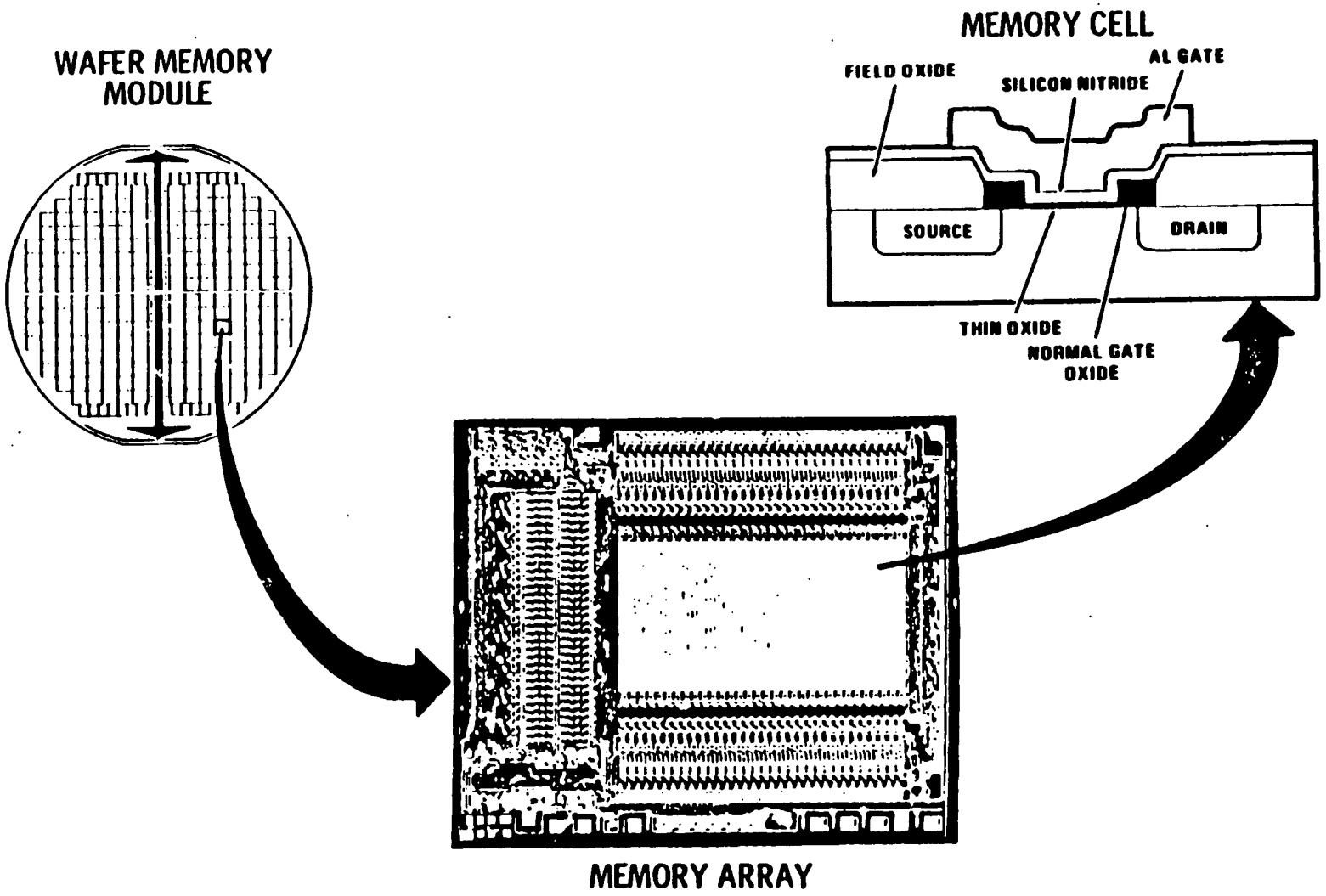
ASSOCIATIVE INTERCONNECTION CIRCUIT



United States Patent **4,188,670** **Feb. 12, 1980**

Inventor: **Yukun Hida**

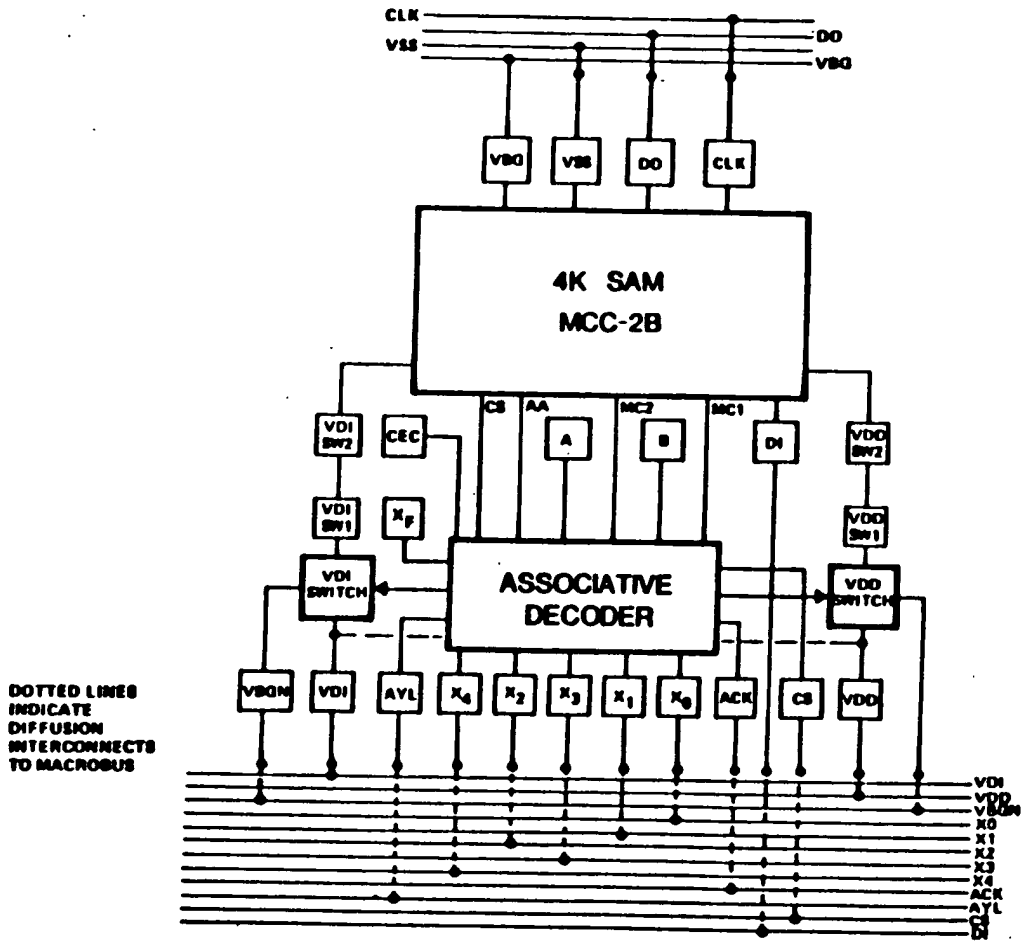
ADAPTIVE WAFER SCALE INTEGRATION APPLIED TO SEQUENTIAL ACCESS MEMORY



LEX08562

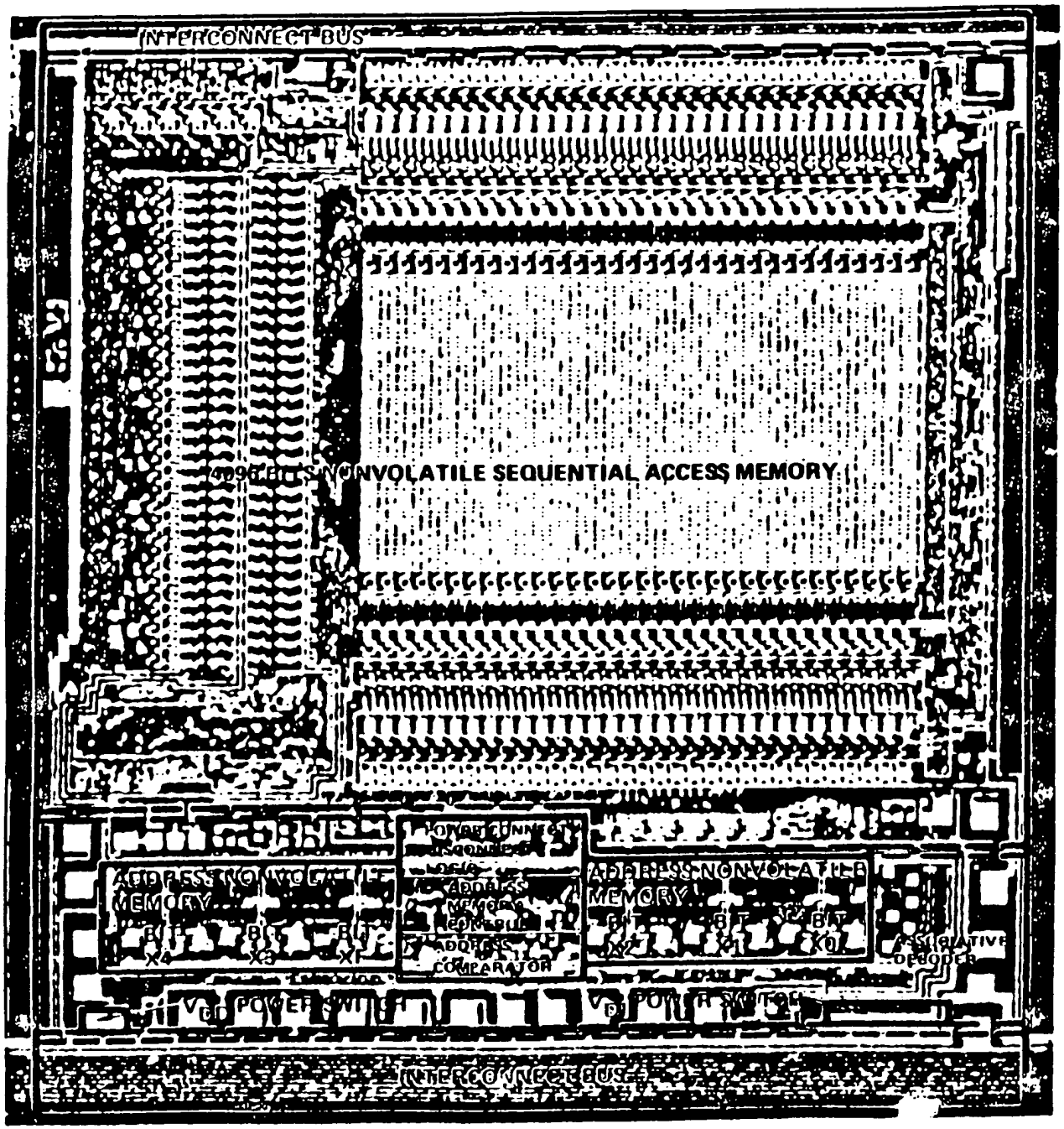
MAW-1 OVERVIEW

ASSOCIATIVE DECODER, MCC-2B WITH INTERNAL PADS, AND MACROBUS



LEX08563

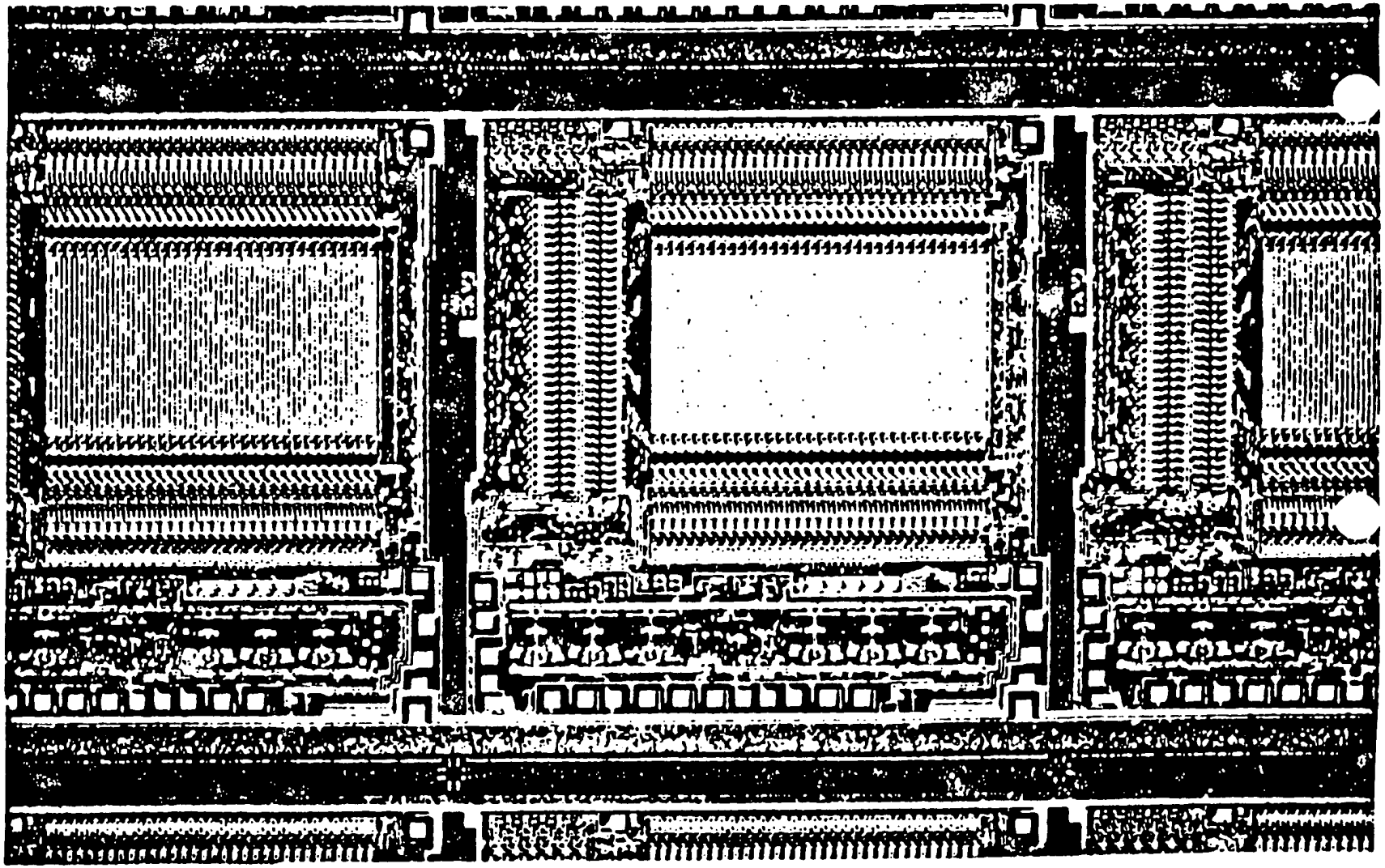
870-AWBI-81041



LEX08564

THE ASSOCIATIVE DECODER, THE MCC-2B MEMORY AND THE INTERCONNECT BUS IN THE MAW-1

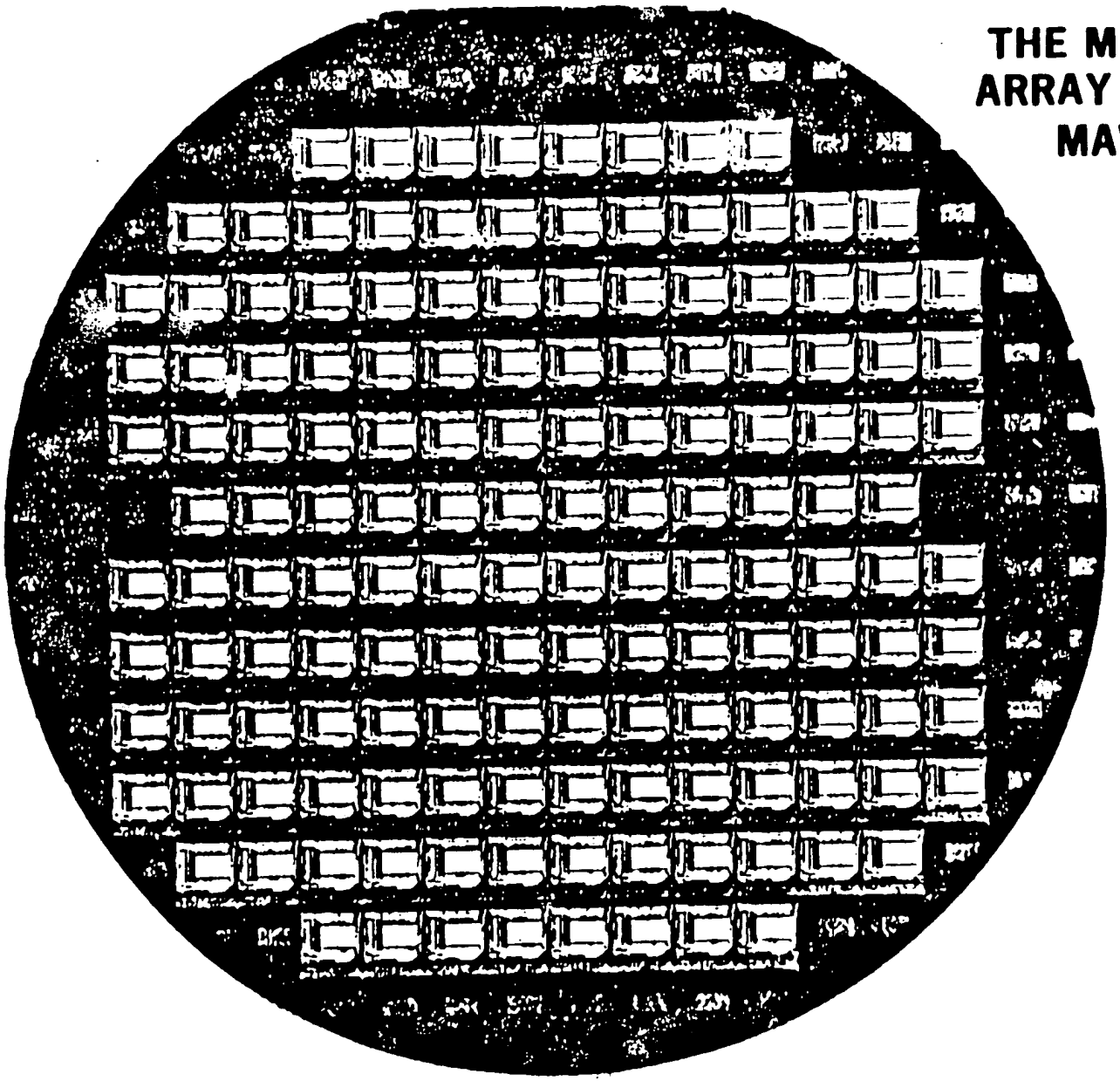
THE WAFER-LEVEL INTERCONNECTED MCC-2B MEMORY ARRAYS



LEX08565

52217

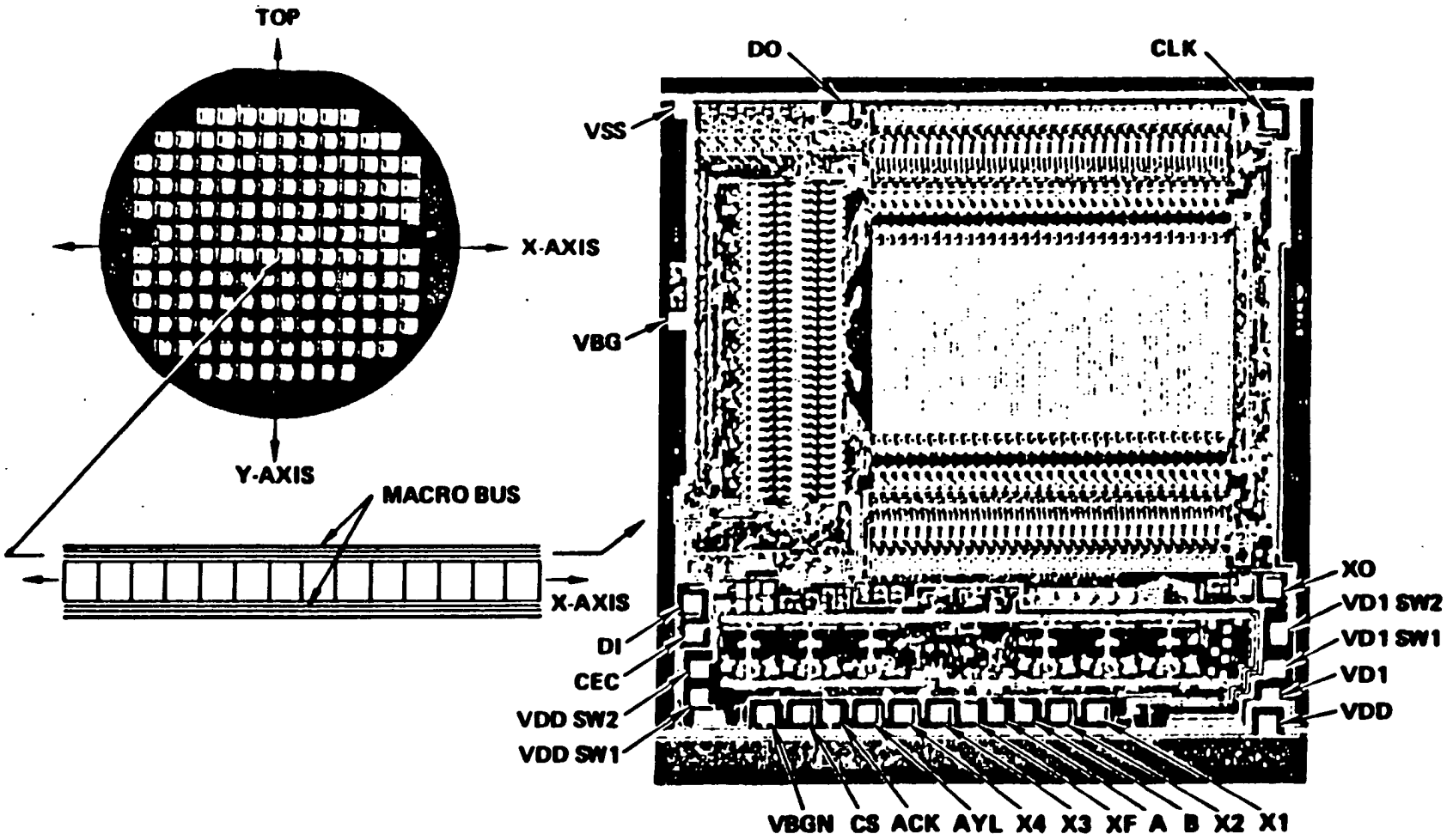
THE MEMORY ARRAY WAFER MAW-1



LEX08566

56148

MAW-1 WAFER TOPOGRAPHY



LEX08597

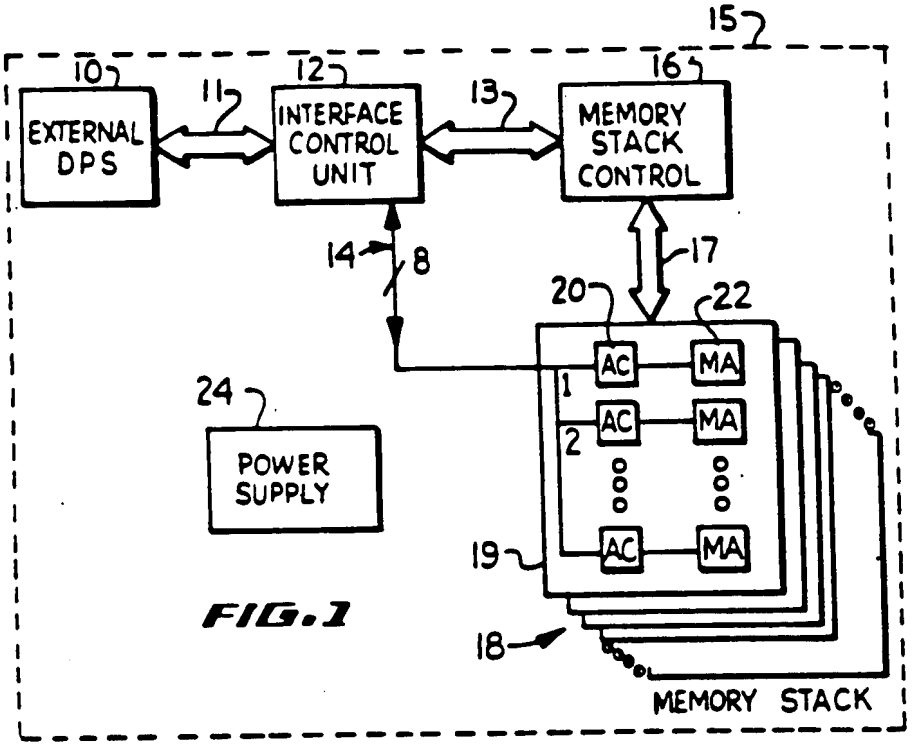


FIG. 1

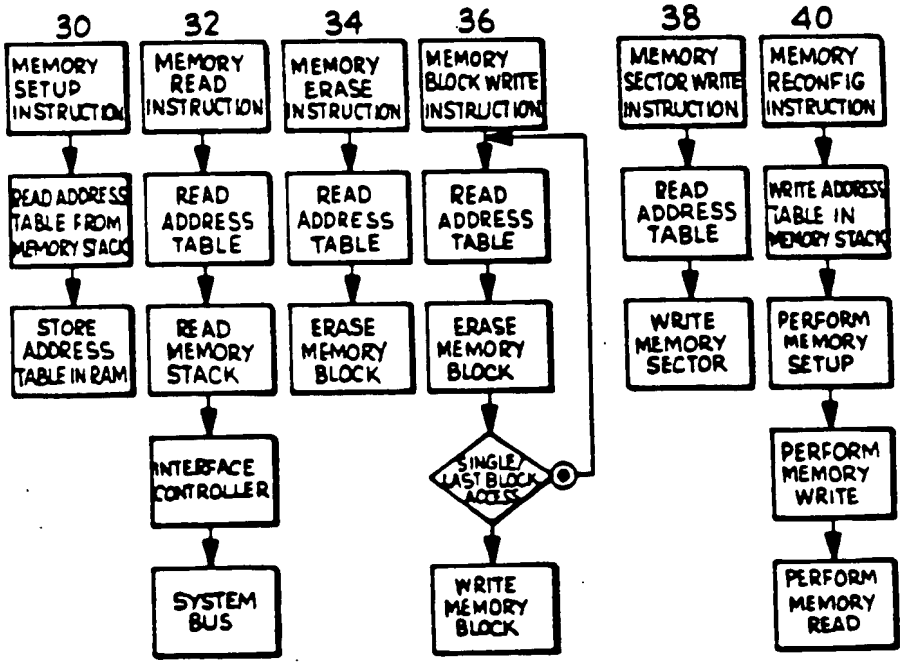
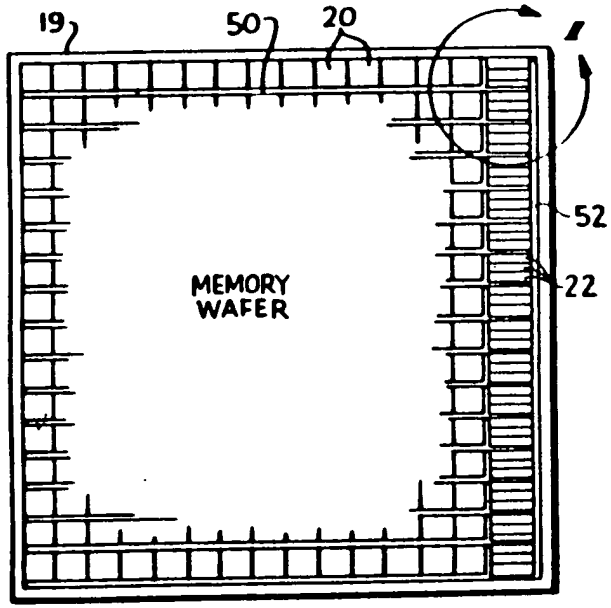


FIG. 2

Inventors: Yukun Hsia; Richard W. Rodgers



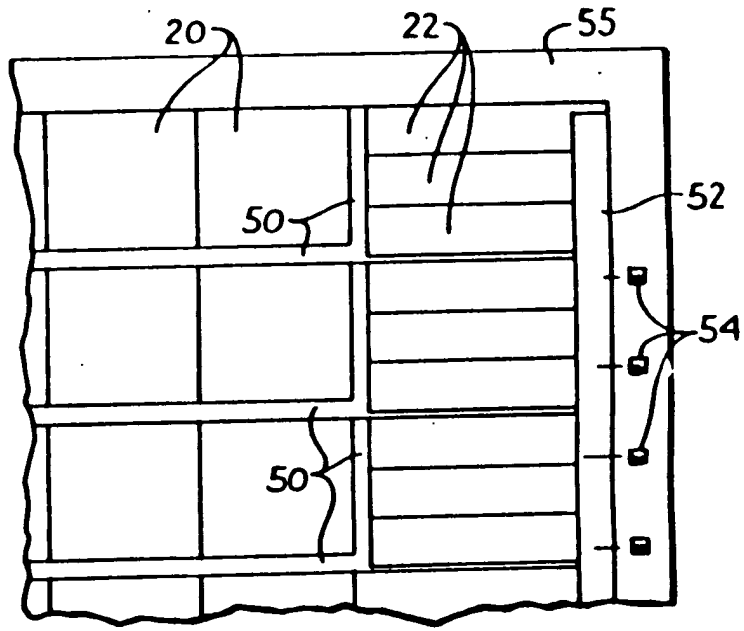
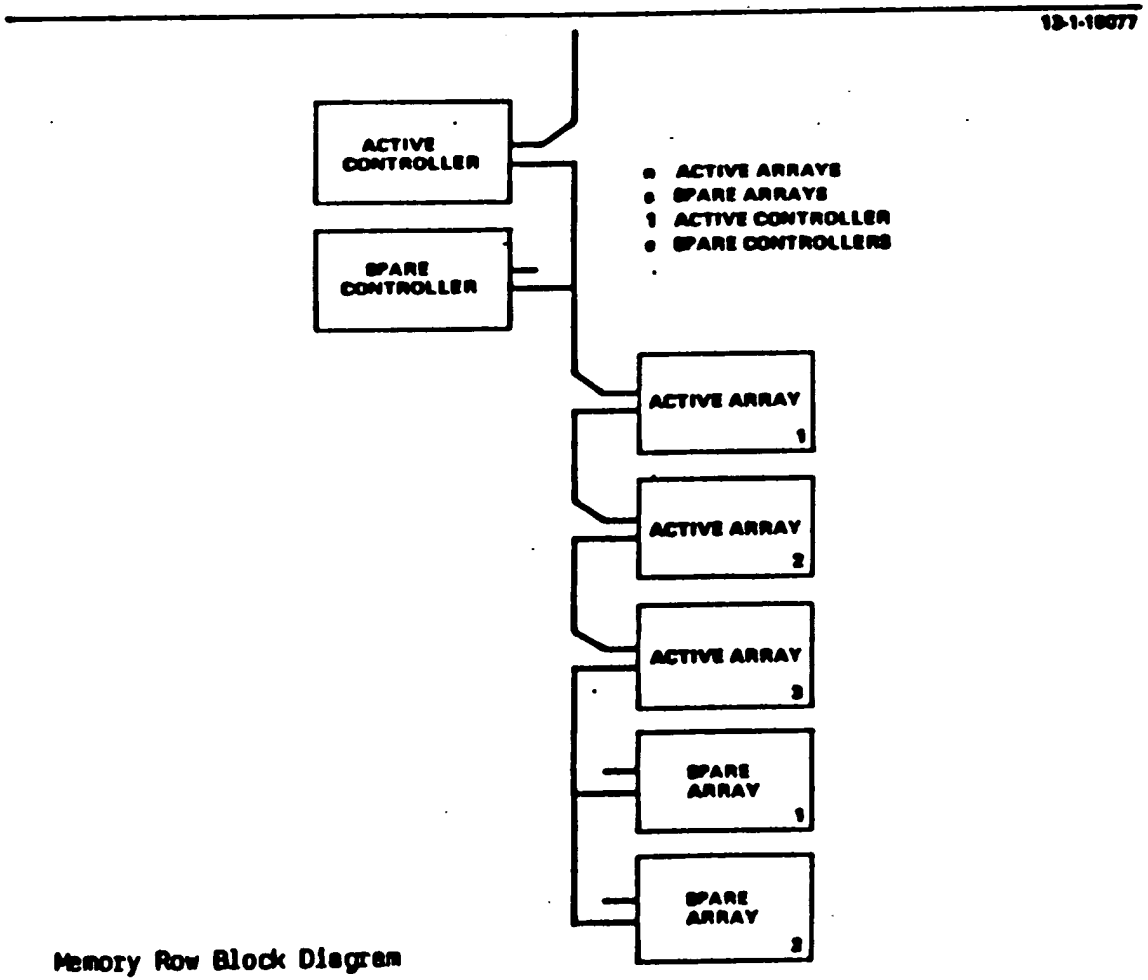


FIG. 1

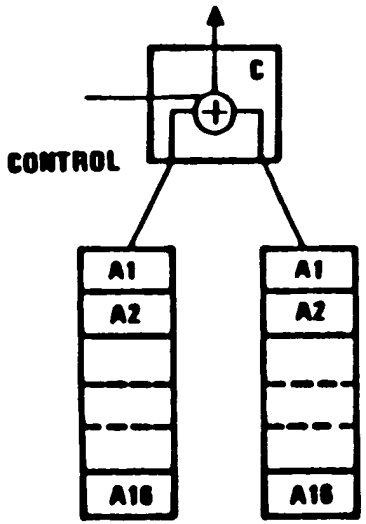
LEX08569



Memory Row Block Diagram

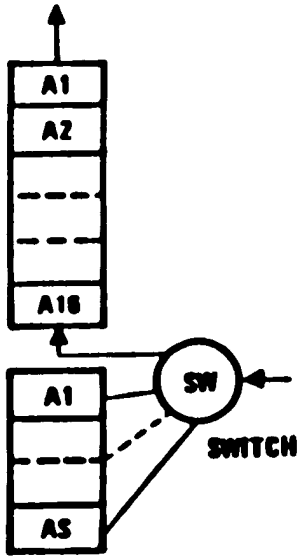
LEX08570

EXAMPLE OF GAIN IN RELIABILITY WITH THE USE OF SPARING REDUNDANCY



DUAL REDUNDANT NETWORK

RELIABILITY	0.9144/5 YRS
FAILURE RATE	0.2%/1000 HRS



SPARING NETWORK

RELIABILITY	0.99858/5 YRS FOR 2 SPARES
FAILURE RATE	0.026%/1000 HRS
RELIABILITY	0.99989/5 YRS FOR 4 SPARES
FAILURE RATE	0.023%/1000 HRS

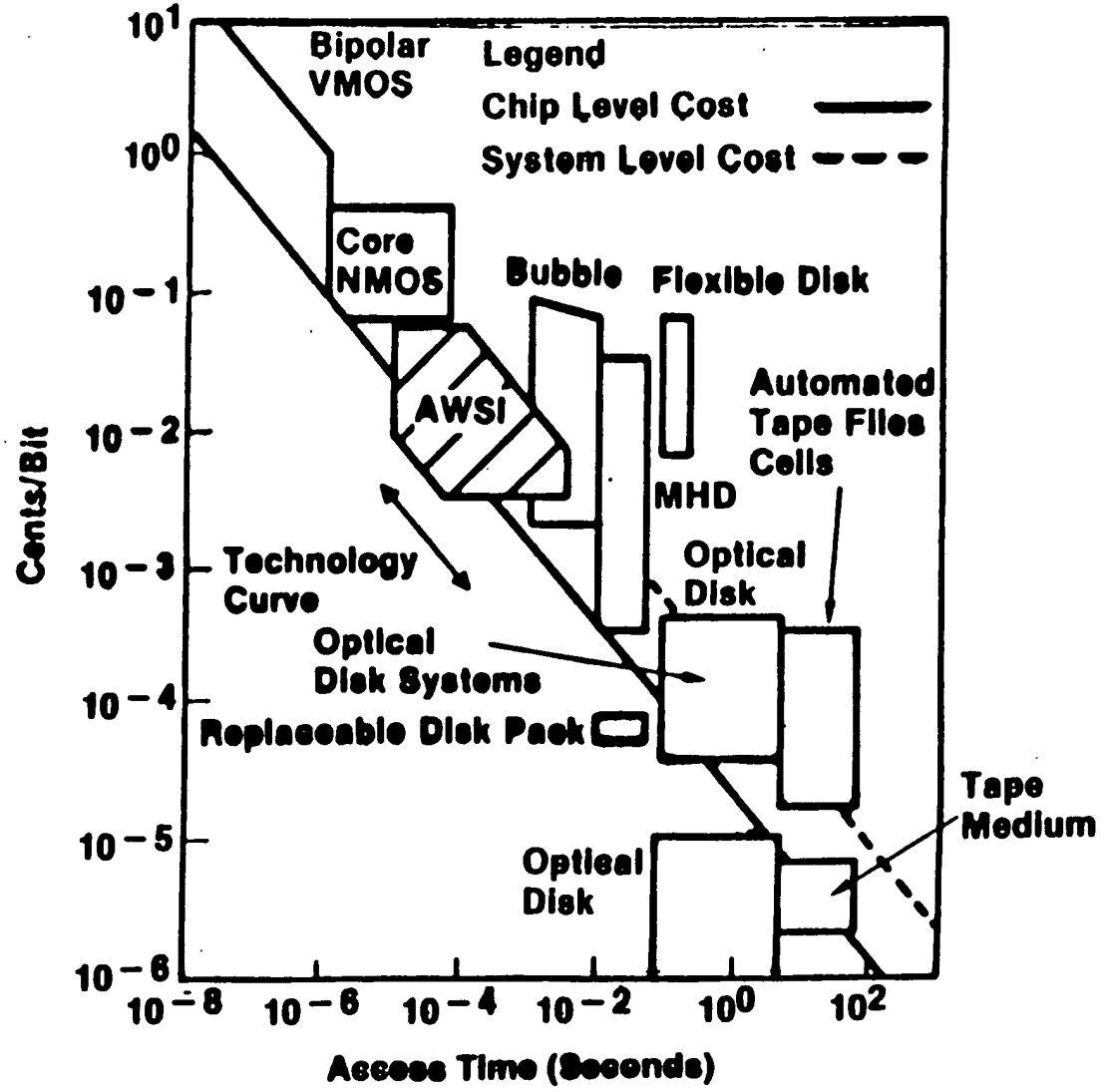
LEX08571

570-AWSI-70440

AWSI MASS MEMORY APPLICATION

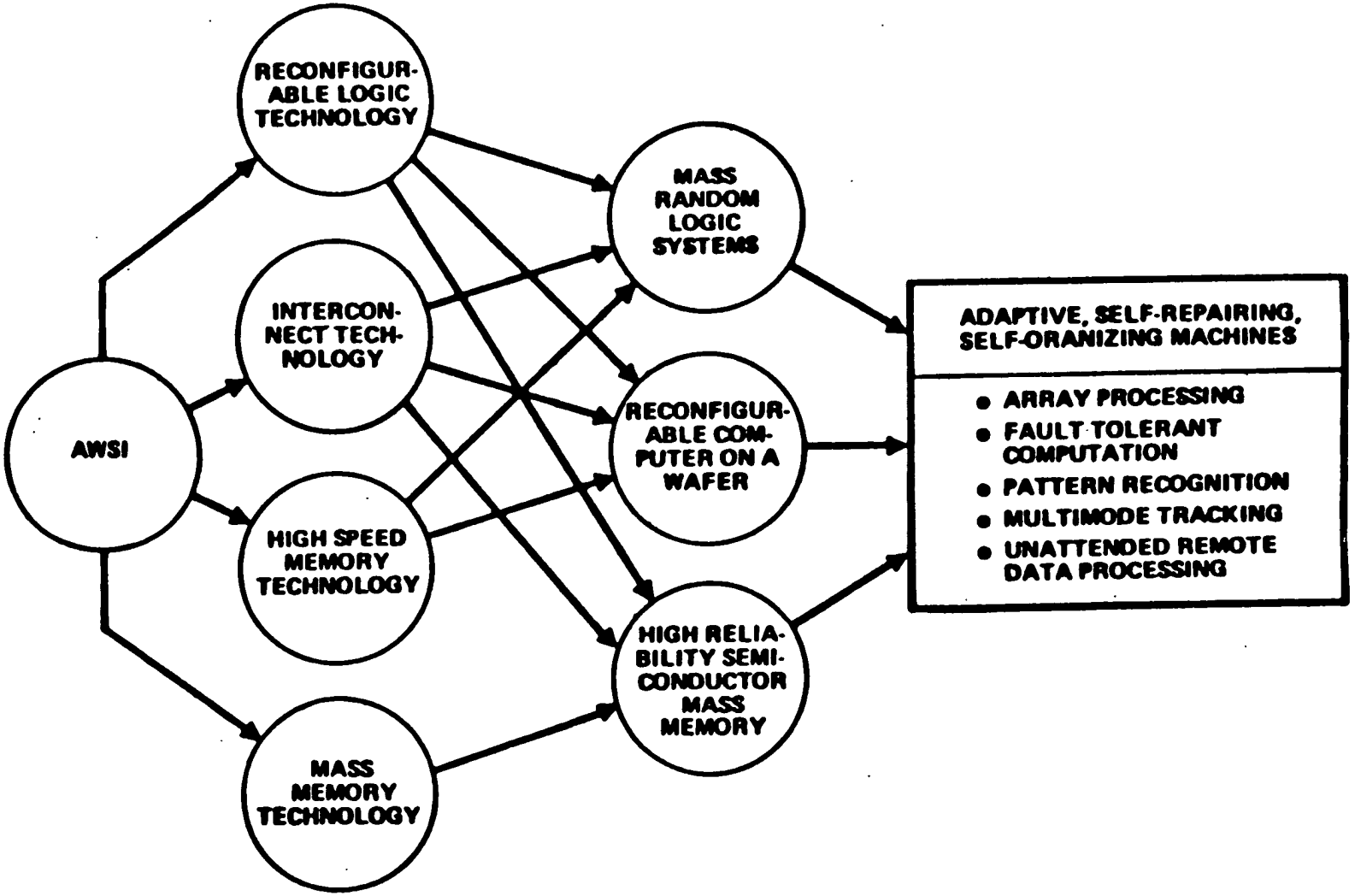
- NONVOLATILE SEMICONDUCTOR STORAGE
- SIGNIFICANT ADVANTAGES IN POWER, VOLUME AND WEIGHT
- HIGH RELIABILITY
  - SPARING REDUNDANCY
  - SELF-REPAIRING
  - RECONFIGURABLE
- LOW LATENCY TIME FOR DATA ACCESS
- HIGH DATA RATE

THE AWSI/MNOS SOLID-STATE MEMORY IN THE STORAGE HIERARCHY



LEX08573

ADAPTIVE WAFER SCALE INTEGRATION OVERVIEW



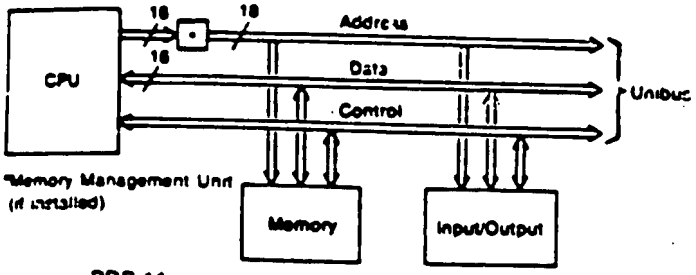
LEX08574

SILICON MACHINE

AN ADAPTIVE, RECONFIGURABLE COMPUTER

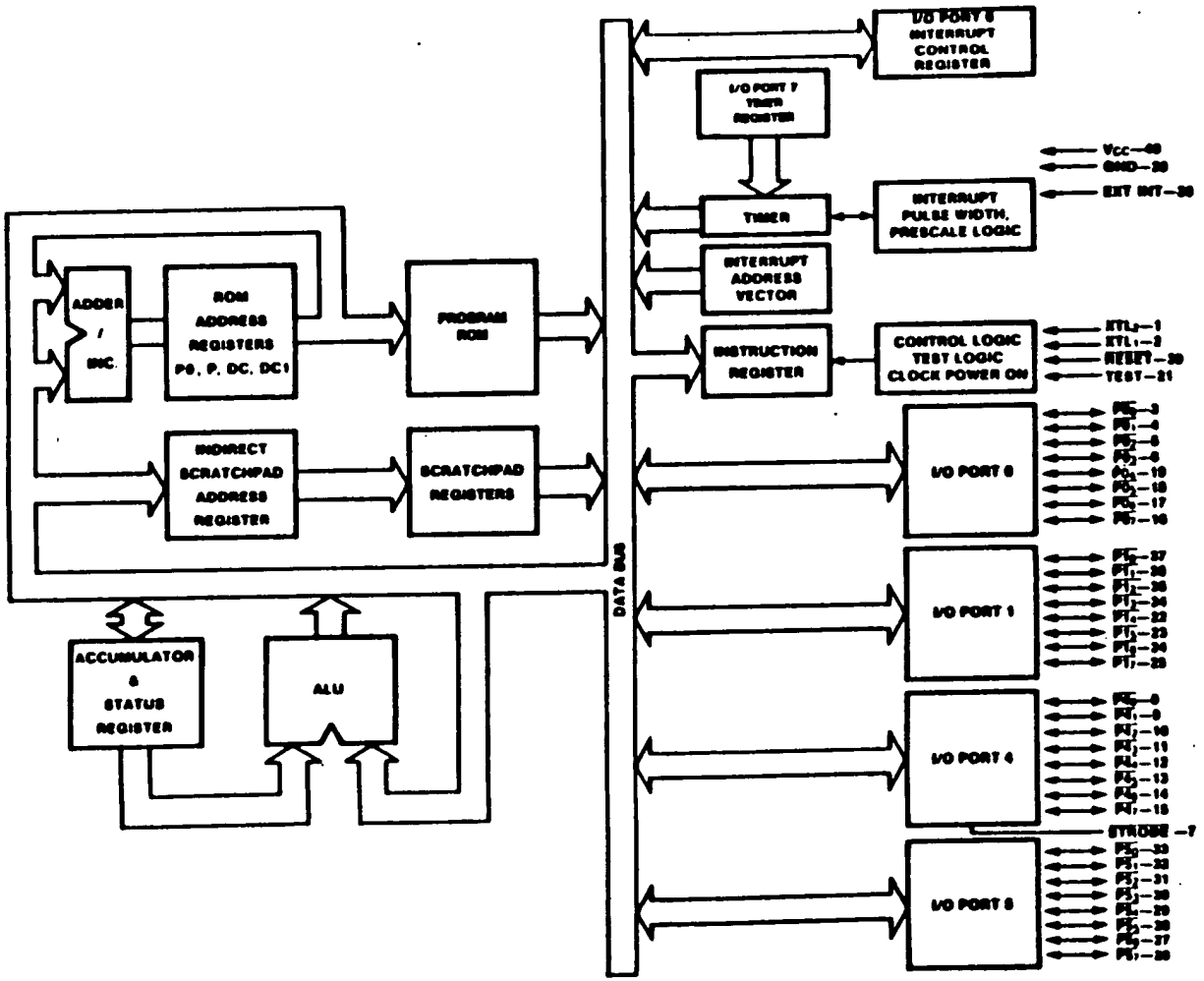
YUKUN HSIA
MARCH 1983
GRADUATE SEMINAR
UNIVERSITY OF
SANTA CLARA

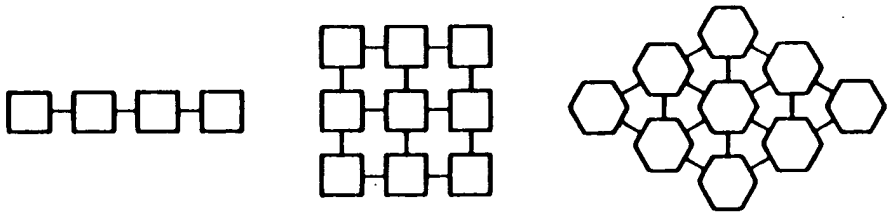
- INTRODUCTION
  - COMPUTER AS AN INTERCONNECT ARCHITECTURE
  - COROLLARY OF ARCHITECTURE
- A FIRST LOOK AT A FIRST ORDER SILICON MACHINE
  - THE WAFER MEMORY
  - FEATURES AND APPLICATIONS
- TECHNOLOGY CONSTRAINTS
  - REVIEW OF PROGRESS
  - PROSPECTS FOR FUTURE



PDP-11 computer block diagram.

F3870 Block Diagram





(a) Linearly connected (b) Orthogonally connected (c) Hexagonally connected

Fig. Mesh-connected processor arrays.

WASP—WAfer-scale Systolic Processor

Kye S. Hedlund
Department of Computer Science
Univ. of North Caroline at Chapel Hill

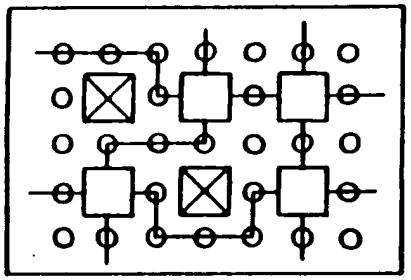


FIGURE 1. Wafer scale systems will require routing around faulty processors.

	Wafer Diameter 4"	6"
Grid size (building blocks)	11 x 11	14 x 14
Fraction of wafer area used	.786	.813
Success rate of structuring algorithm	.957	.931
Mesh dimensions (PEs)	22 x 22	28 x 28
PEs per wafer	484	784

TABLE 1. Characteristics of the WAfer-scale Systolic Processor (WASP).

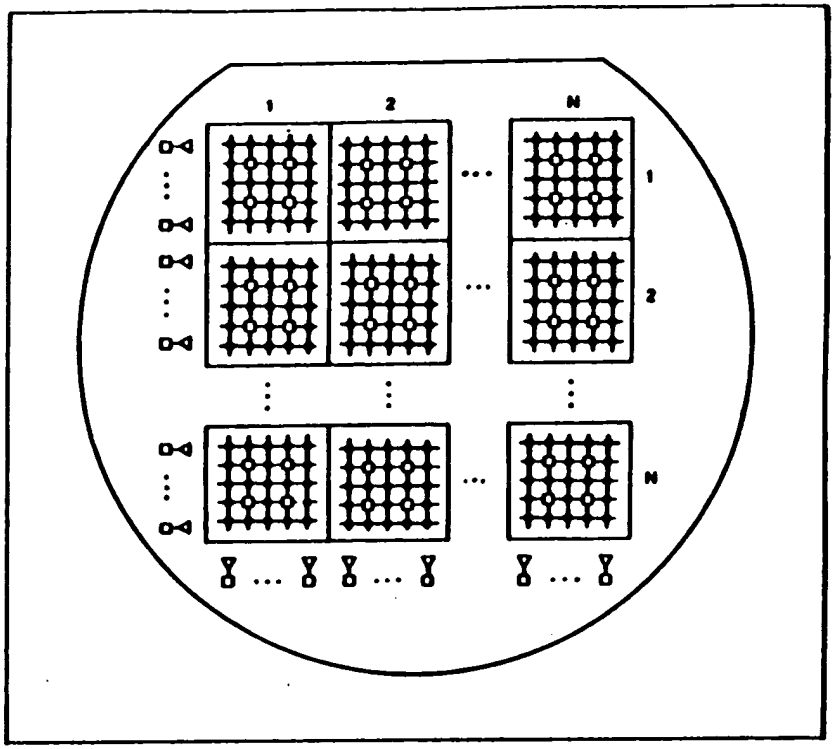


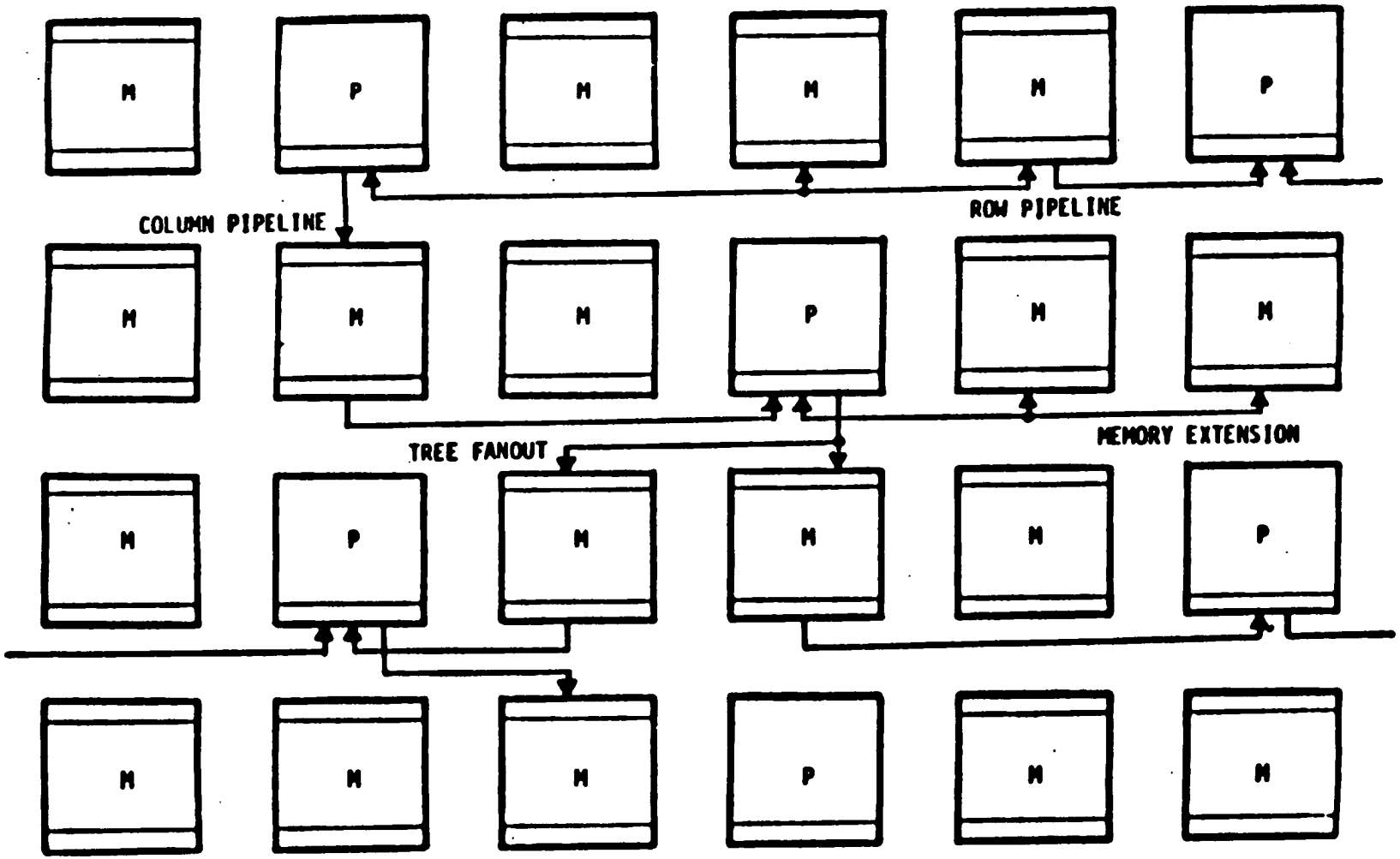
FIGURE 2. Squares are PEs; circles are switches; bonding pads and drivers shown on wafer edge.

The characteristics of a PE are:

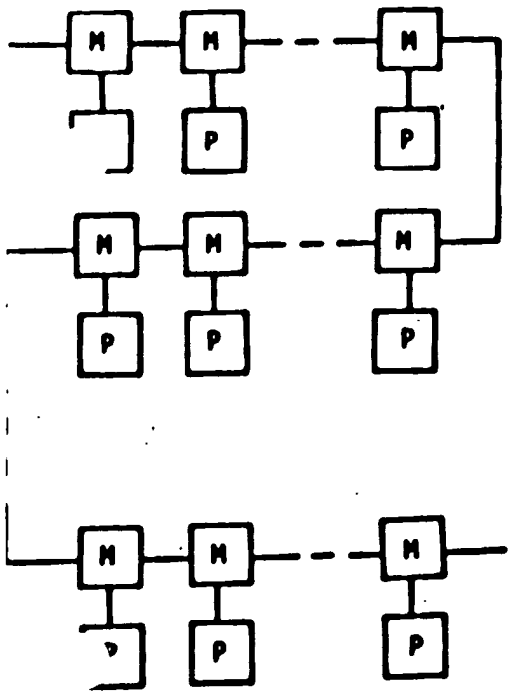
1) Simple, arithmetic-oriented instruction set
2) 8-bit ALU
3) 64 bytes of program memory
4) 16-byte register file
5) Four data ports for communicating with neighbors

THE SILICON MACHINE -

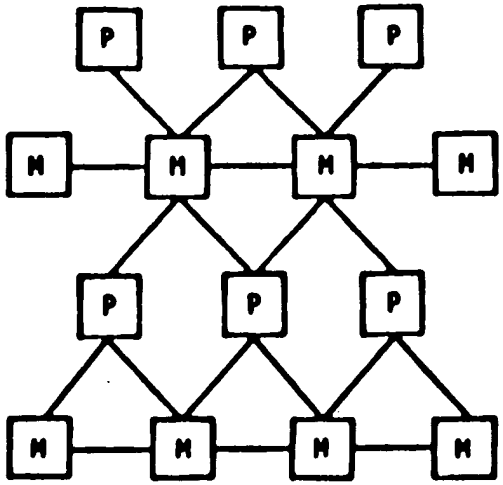
SYSTEM INTERCONNECT EXAMPLES



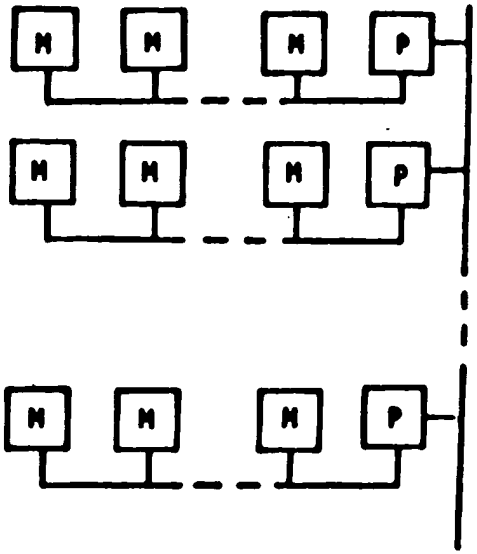
THE SILICON MACHINE ARRAY NETWORK



PIPELINE PROCESSING



TREE ARCHITECTURE



MASS MEMORY TOPOLOGY

LEXMRK1

REQUIREMENTS OF TECHNOLOGY IMPOSED BY THE SILICON MACHINE ARCHITECTURE

- NON-VOLATILE CONFIGURATION
- IN-SITE ALTERABLE INTERCONNECT
- NON-VOLATILE ALTERABLE MEMORY
- VLSI, VLSI/WSI PACKAGING

TECHNOLOGY CONSTRAINTS/CHALLENGES

(1)	PROCESS	VLSI	POWER DISSIPATION CMOS, PACKAGING
			INTERCONNECT RELIABILITY ELECTROMIGRATION
		NVSM	MNOS, EEPROM
(2)	DESIGN	YIELD	
		YIELD-LIMITED DESIGN	
		BUILT-IN-DIAGNOSTICS	
		BUILT-IN-TESTS	
(3)	SYSTEM	INTERCONNECT MANAGEMENT	
		SYSTEM ARCHITECTURE DEVELOPMENT	

LEX08583

COROLLARY OF SILICON MACHINE ARCHITECTURE

- EMPHASIS ON INSTRUCTION AND DATA FLOW
- CELLULAR DESIGN FOR ORDERED INTERCONNECT
- SYSTEM CONFIGURABILITY WITH INTERCONNECT
  - RECONFIGURABLE COMPUTER

COROLLARY OF SILICON MACHINE ARCHITECTURE

- RECONFIGURABLE COMPUTER
  - LOW COST CUSTOMIZATION
  - SPARING REDUNDANCY
    - WAFER-SCALE INTEGRATION
    - GRACEFUL DEGRADATION
  - SELF-REPAIRING
    - HIGHLY RELIABLE ELECTRONIC SYSTEMS
  - ADAPTIVE PROCESSING
  - ARTIFICIAL INTELLIGENCE

PROSPECTS FOR SILICON MACHINE

NEAR-TERM APPLICATIONS

UNMANNED SYSTEMS

ROBOTICS

FUTURE

INTELLIGENT MACHINES FOR AUTOMATED FACTORY

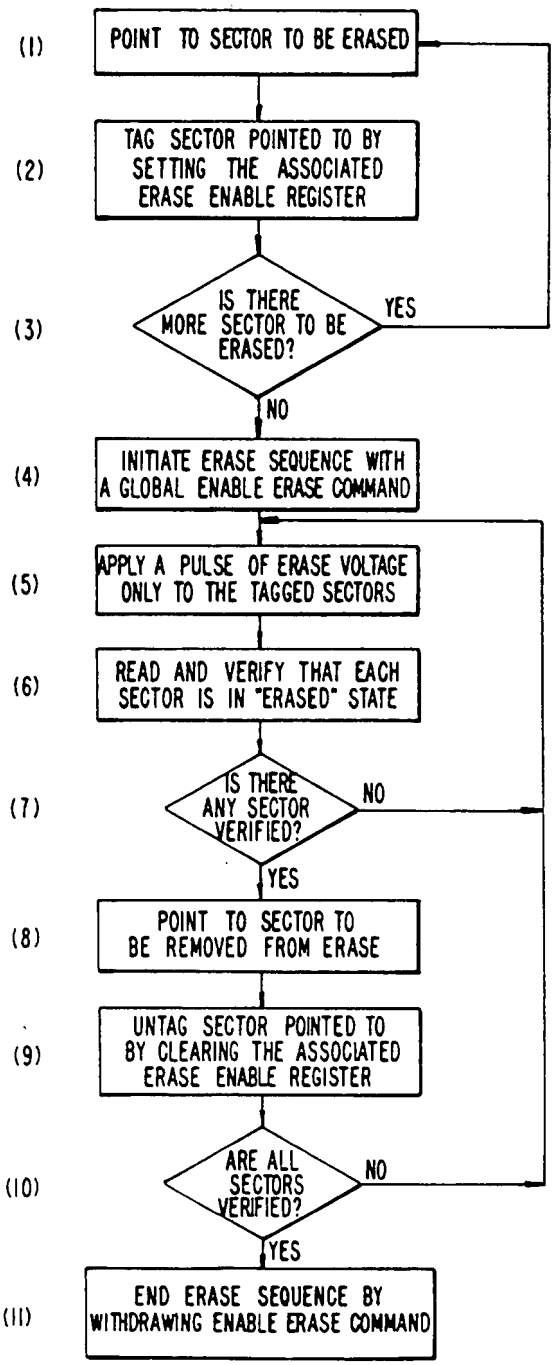
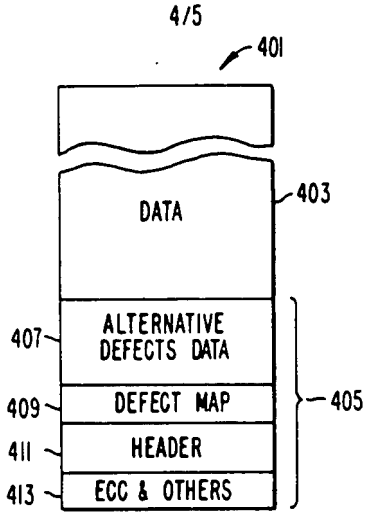

(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
NO
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED?
NO
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG._4.



SECTOR PARTITION

FIG._5.

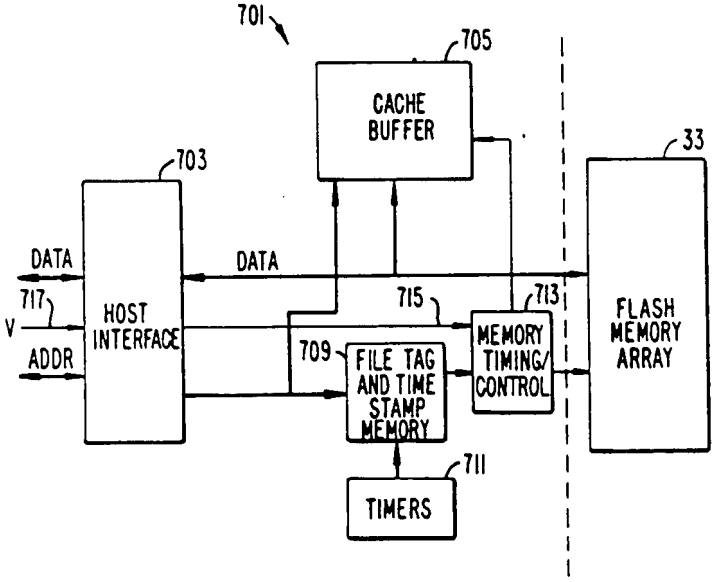
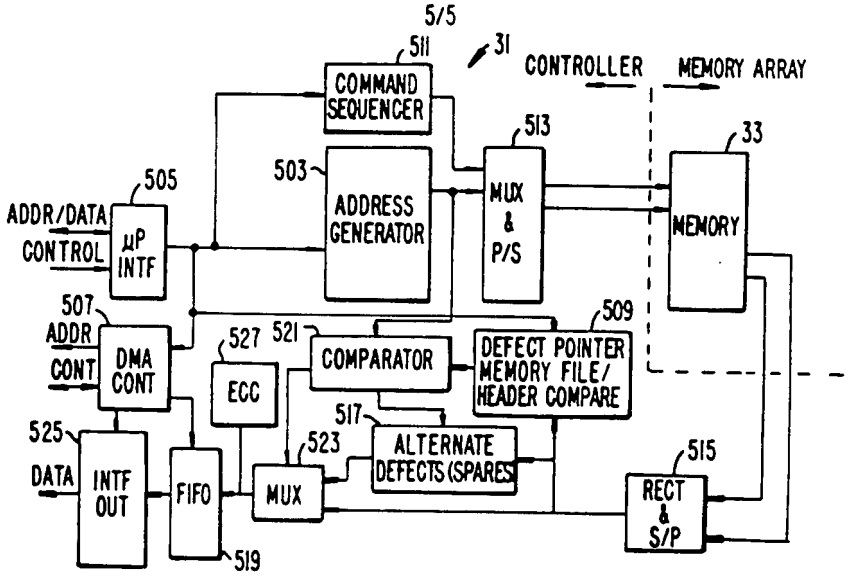
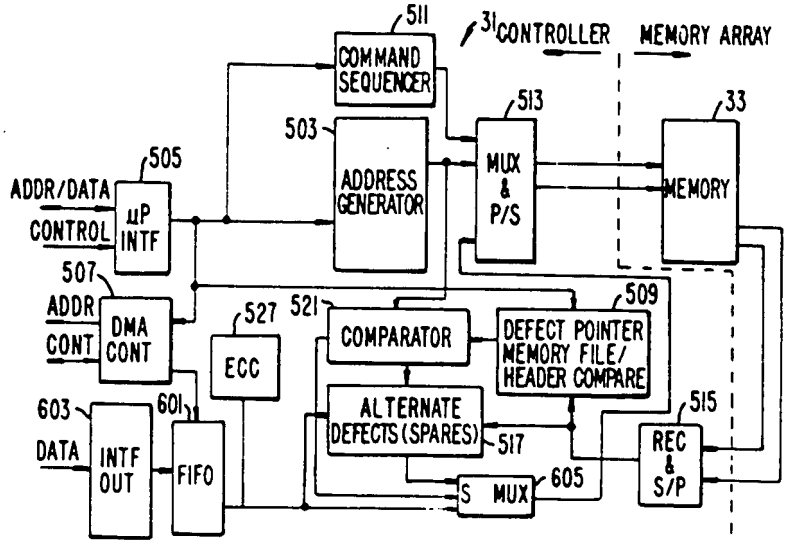


FIG._8.



READ DATA PATH CONTROL

FIG._6.



WRITE DATA PATH CONTROL

FIG._7.

142 - 1,290.00
541 - 130.00

PART B—ISSUE FEE TRANSMITTAL

MAILING INSTRUCTIONS: This form should be used ... transmitting the ISSUE FEE. Blocks 2 through 6 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to addressee entered in Block 1 unless you direct otherwise, by: (a) specifying a new correspondence address in Block 3 below; or (b) providing the PTO with a separate "FEE ADDRESS" for maintenance fee notifications with the payment of Issue Fee or thereafter. **See reverse for Certificate of Mailing.**

1. CORRESPONDENCE ADDRESS	2. INVENTOR(S) ADDRESS CHANGE (Complete only if there is a change)
24M1/0820 GERALD P. PARSONS MAJESTIC, PARSONS, SIEBERT & HSUE FOUR EMBARCADERO CENTER, SUITE 1450 SAN FRANCISCO, CA 94111-4121	INVENTOR'S NAME Street Address City, State and ZIP Code CO-INVENTOR'S NAME Street Address City, State and ZIP Code ☐ Check if additional changes are on reverse side

OCT 15 1996

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/174,768	12/29/93	050	HUA, L 2813	08/20/96

First Named Applicant: HARARI, ELIYAHOU

TITLE OF INVENTION: FLASH EEPROM SYSTEM

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2	HARI0606	395-182.060	024	UTILITY	NO	$1250.00	11/20/96

3. Correspondence address change (Complete only if there is a change)
Majestic, Parsons, Siebert & Hsue
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111

4. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will be printed.
1 Majestic, Parsons, Siebert & Hsue
2
3

DO NOT USE THIS SPACE

840 BL 1:12+:98 08:174768
1 142 1,290.00 CR
1 30: 30.00 CR

5 ASSIGNMENT DATA TO BE PRINTED ON THE PATENT (print or type)
(1) NAME OF ASSIGNEE
SanDisk Corporation
(2) ADDRESS (CITY & STATE OR COUNTRY)
Sunnyvale, California

A ☐ The application is NOT assigned
☒ Assignment previously submitted to the Patent and Trademark Office
☐ Assignment is being submitted under separate cover. Assignments should be directed to Box ASSIGNMENTS
PLEASE NOTE. Unless an assignee is identified in Block 5, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

6a. The following fees are enclosed:
☒ Issue Fee ☒ Advance Order - # of Copies 10
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DEPOSIT ACCOUNT NUMBER 13-1030
(ENCLOSE PART C)
☐ Issue Fee ☐ Advance Order - # of Copies
☒ Any Deficiencies in Enclosed Fees

The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified above.

(Authorized Signature) [signature] (Date) Oct. 9, 1996

NOTE: The Issue Fee will not be accepted from anyone other than the applicant, a registered attorney or agent, or the assignee or other party in interest as shown by the records of the Patent and Trademark Office

TRANSMIT THIS FORM WITH FEE-CERTIFICATE OF MAILING ON REVERSE

PTOL-85B (REV 4-94) (0651-0033)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
ELIYAHOU HARARI et al.	Group Art Unit: 2413
Serial No.: 08/174,760	Examiner: L. Hua
Filed: December 29, 1993	
For: FLASH EEPROM SYSTEM	San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on October 8, 1996.

Brenda J. Dolly

Brenda J. Dolly Oct. 8, 1996

Signature Date

NOTICE OF CHANGE OF ADDRESS FOR ASSIGNEE

Sir:

Please take notice that the assignee of record in the above-identified application has moved their offices to the address listed below:

SanDisk Corporation
140 Caspian Court
Sunnyvale, California 94089

Dated: October 8, 1996

Respectfully submitted,

Philip Yau, Reg. No. 32,892
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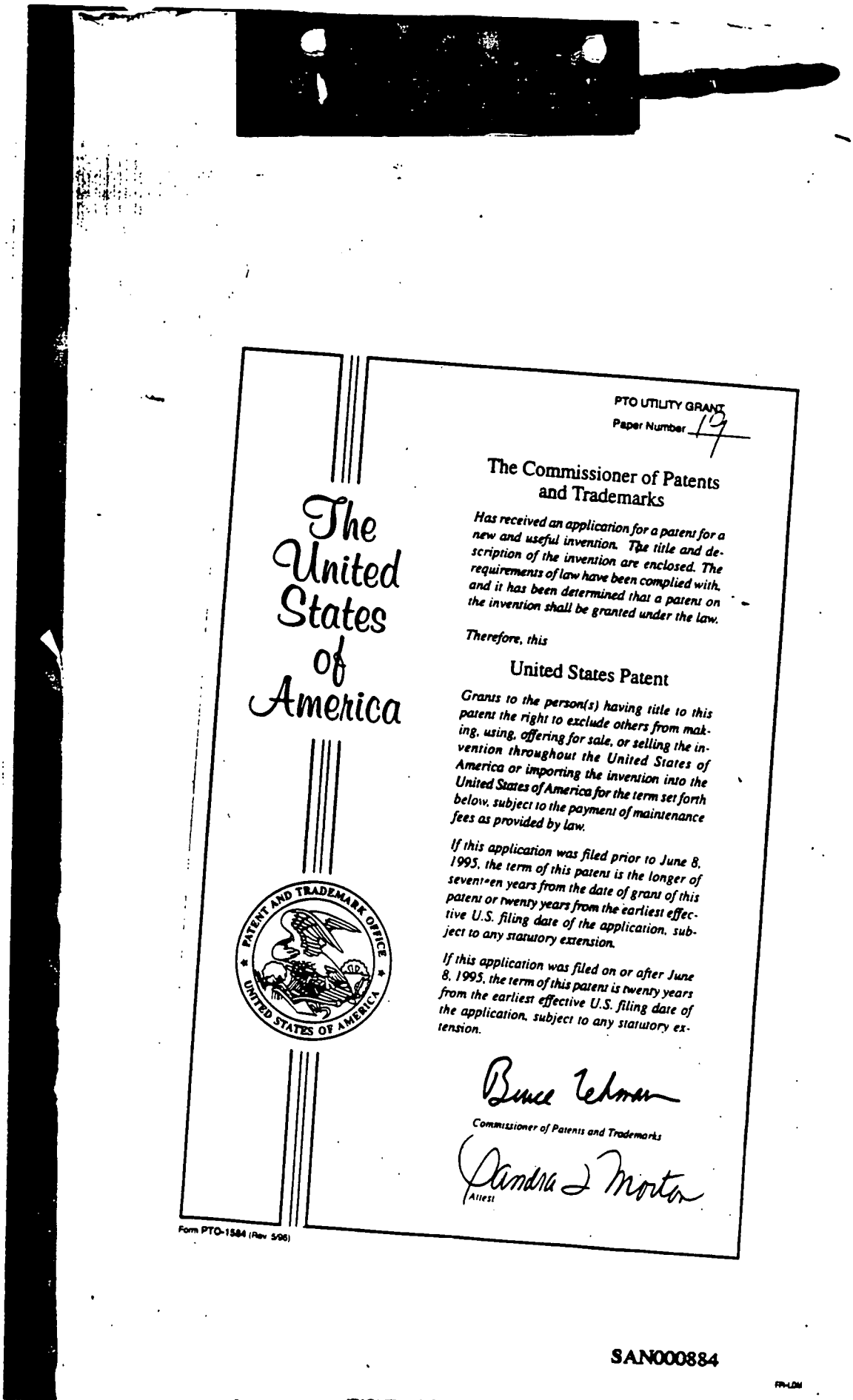
Atty. Docket: HARI.006US6

SAN000882



PTO UTILITY GRANT
Paper Number 19

The United States of America

The Commissioner of Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

Bruce Lehman

Commissioner of Patents and Trademarks

Sandra L Morton

Attest

Form PTO-1584 (Rev. 5/96)

SAN000884

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